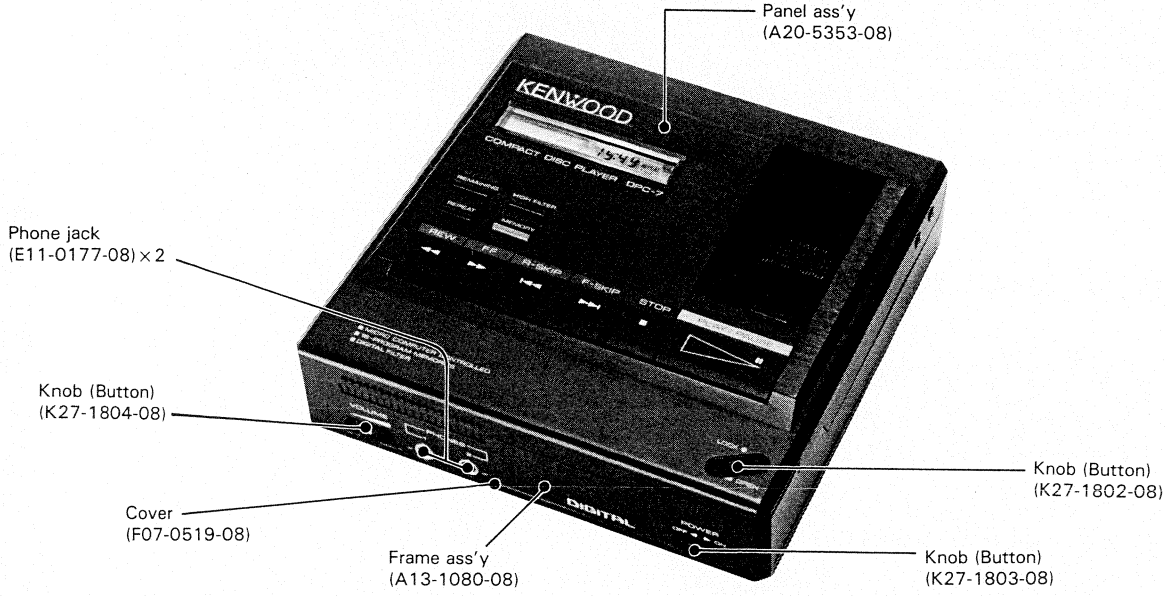
COMPACT DISC PLAYER

DPC-7

SERVICE MANUAL

KENWOOD

B51-3260-00(T)485



SPECIFICATIONS

PICK UP

Type.....Optical Pick Up
Laser Type.....Semiconductor Laser

AUDIO

Channels.....2 Channels
Frequency Response.....20 Hz-20 kHz, ±1 dB
Dynamic Range.....90 dB at 1 kHz
Total Harmonic Distortion.....0.05% at 1 kHz
Channel Separation.....85 dB at 1 kHz
Wow & Flutter.....Unmeasureble Limit
Line Output Level/Impedance...1.0 V/16 ohms
Headphones Output Level.....20 mW + 20 mW (at 16 ohms)

GENERAL

Power Requirements.....DC : 6 V (Supplied Lead-acid Batteries)
AC : (Supplied AC Adaptor)
110-120 V/220-240 V, 50/60 Hz
(Other countries)
220 V/50 Hz (Europe Medels)
120 V/60 Hz
(U.S.A. & Canada Models)
Power Consumptions.....1.8 W
Battery Life.....Approx. 6 Hours (Supplied Lead-acid Batt.)
Dimentions.....126 (W) × 29.8 (H) × 126 (D) mm
4-31/32″ (W) × 1-3/16″ (H) × 4-31/32″ (D)
Weight.....520 g (Without Battery Pack)
910 g (With Battery Pack)
Supplied Accessories.....Lead-acid Rechargeable Battery Pack
(Charging time; Approx. 8 Hours)
AC Adaptor (Useable Battery Charger)
Carring Case
Carring Belt
Car Audio Cassette Adaptor

KENWOOD follows a policy of continuous advancements in development.
For this reason specification may be changed without notice.

DANGER
INVISIBLE LASER RADIATION WHEN OPEN AND INTERLOCK DEFEATED. AVOID DIRECT EXPOSURE TO BEAM.

* Refer to parts list on page 73.

DPC-7

CONTENTS

PRECAUTION FOR HANDLING LASER PICKUP

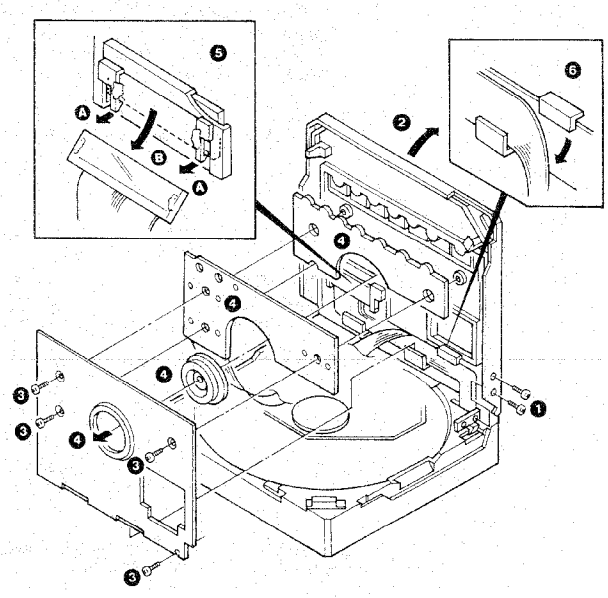
The pickup used in this unit is easily damaged by static electricity. Take careful note of the following points when soldering and handling this divice.

1. Make sure to first discharge yourself to ground.
2. Use a grounded-tip soldering iron.
3. Ground the divice while soldering in.
4. Cover the work table with conductive, grounded panel to insure an adequate static discharge path.

Don't open the divice of repairing parts from the anti-static bag, if not necessary.

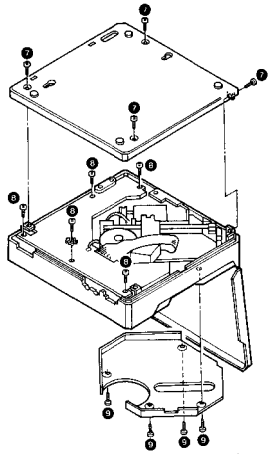
DISASSEMBLY FOR REPAIR

1. Remove the two screws fixing the panel ass'y to the arm (No.215 in the Unit Exploded View diagram) (❶).
2. Lift the panel ass'y up in the direction of the arrow (❷).
3. Remove the four screws fixing the holder (No.243 in the Unit Exploded View diagram) to the panel ass'y (❸).
4. Remove the holder (clamp), Switch Unit (X13-5770-00), and rubber sheet (❹).
5. Remove the adhesive holding the panel to the (LCD) window ass'y (two points), disengage the two claws fixing it (❺ Ⓐ), and remove the LCD window ass'y in the direction of the arrow (❺ Ⓑ).
6. Separate the flexible PC board of the LCD window ass'y from the claw on the panel ass'y (❻).

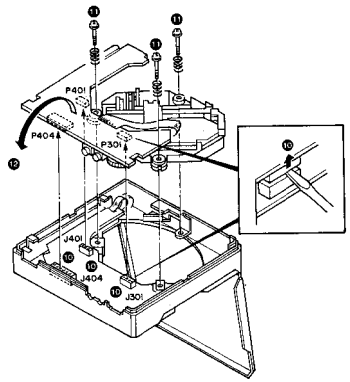


DISASSEMBLY FOR REPAIR

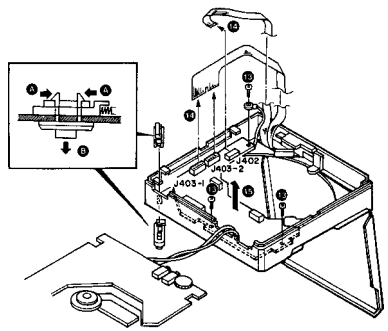
7. Remove the four screws (❼) fixing the cover (bottom case) to the chassis, and remove the cover (bottom case).
8. Remove the five screws fixing the first Auxiliary Unit (X25-3100-00) to the chassis (❽).
9. Remove the four screws fixing the mechanism ass'y cover to the chassis (❾).



10. Using a flat-blade screwdriver, disconnect the connector between one Auxiliary Unit (X25-3100-00) and the other Auxiliary Unit (X25-3090-00) (❿).
11. Remove the three screws and three springs used to fix the mechanism ass'y to the chassis (⓫).
12. Remove the mechanism ass'y, then remove the first Auxiliary Unit (X25-3100-00) in the direction of the arrow (⓬).

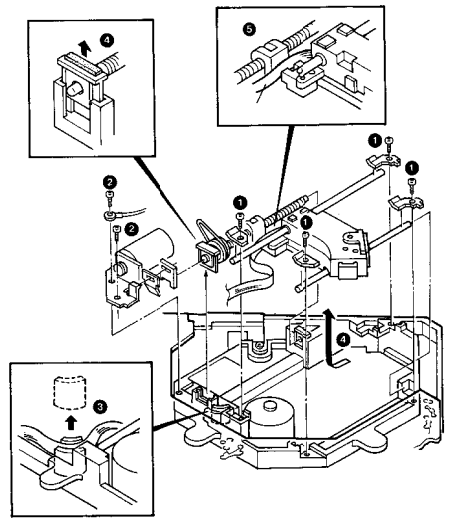


13. Remove the three screws fixing the other Auxiliary Unit (X25-3090-00) to the chassis (⓭).
14. Remove the flexible PC board connected across pin connectors J402, J403-1 and J403-2 (⓮).
15. Remove the other Auxiliary Unit (X25-3090-00) (⓯).
16. Remove the OPEN/CLOSE knob by disengaging the two claws (Ⓐ) and pulling the knob out, as shown in the diagram (Ⓑ).



DISASSEMBLING THE MECHANISM

1. Remove the four clamps retaining the two pickup shafts (❶).
2. Remove the two screws fixing the motor holder to the mechanism chassis ass'y (❷).
3. Remove the EPC clamp (No. 802 in the Mechanism Exploded View diagram), then the flexible PC board held by the clamp (❸).
4. Pull the feed screw ass'y and pickup in the direction of the arrow, and separate the feed screw ass'y and the two slide shafts from the pickup (❹).
5. When assembling the pickup, pay attention to the position of the flexible PC board, as shown by (❺).



1. Feed Motor Current Check

Apply 1.5 V DC to the feed motor and check the current. A feeding operation, from the inner to the outer tracks, shall be performed with a current of about 70 mA.

2. Lead-In Time Check

Measure the time using the SONY test disc (YEDS-18, TYPE 4). The time shall be between 4 min. 30 sec. and 5 min.

The time can be adjusted by the leaf switch position.

3. Leaf Switch Replacement

The leaf switch can be replaced in a way similar to the head replacement, that is, by removing the feed screw and head. Be careful not to spoil the screw thread during this operation.

After replacement, check the lead-in time.

4. Joint Arm Replacement

Follow the same procedure as for the head replacement, then remove the old joint arm from the laser pickup and replace it with a new one. Be careful not to leave adhesive on the laser pickup.

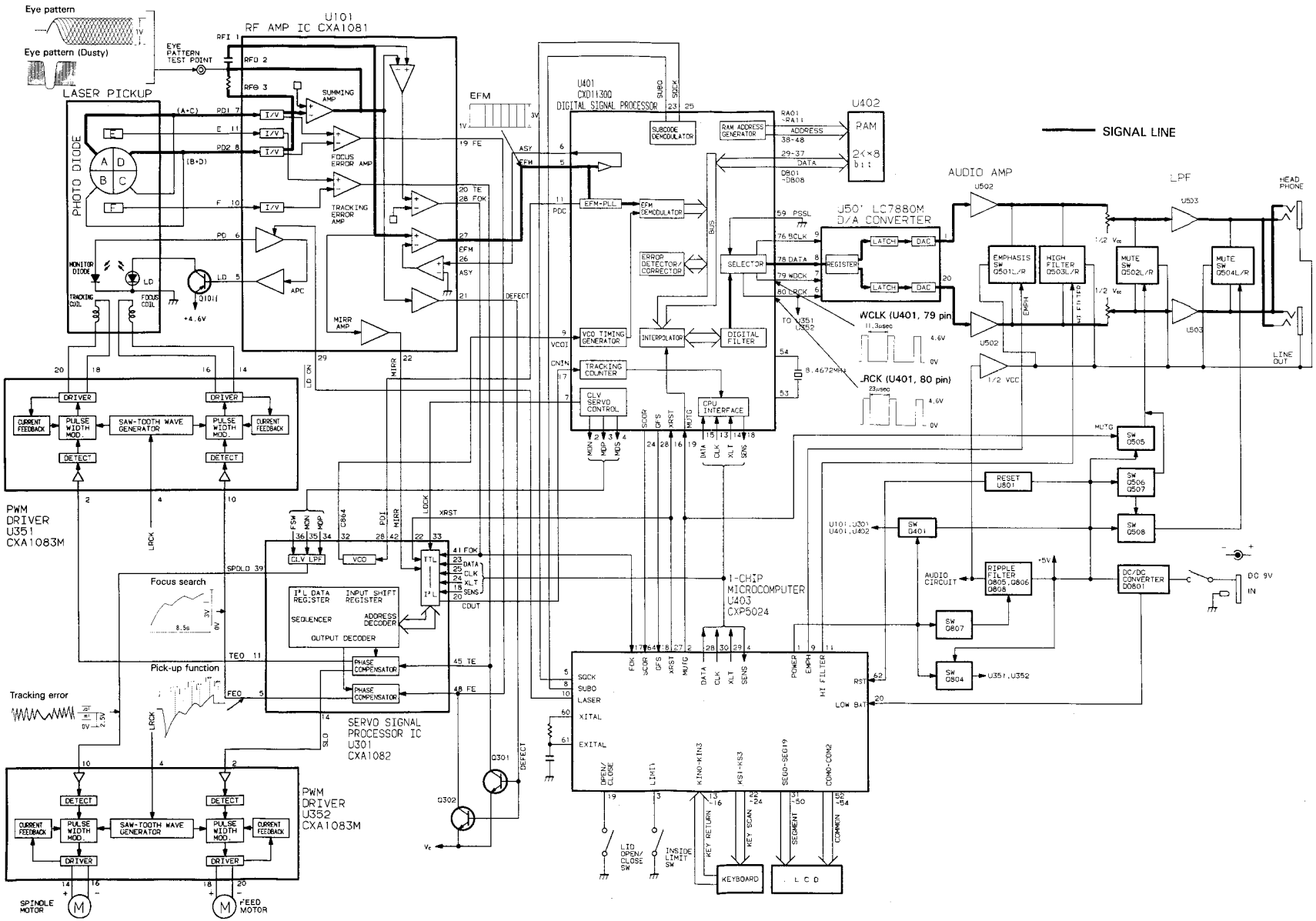
5. Disc Table Replacement (Concerning motor or mechanism chassis)

As the disc table is fastened to the disc motor shaft, these parts shall be replaced as an assembled set.

The parts are also supplied as an assembly.

When replacing, change the entire assembly.

BLOCK DIAGRAM



■ Safety precautions

a) Do not remove the case or disassemble the unit.
b) Do not touch the pickup lens or the mirrored surface of the disc with your finger.
c) Do not drop the unit or subject it to excessive shock.
(If damaged is caused by a drop, it will not be covered under the warranty.)
d) Do not cover or enclose the unit with a cloth, etc.; keep appropriate ventilation.

■ Beware of condensation

- Immediately after a heater is turned on, or in a highly humid place, "dew" may condense on the pickup of this unit and correct operation may be impossible. In this case, turn the POWER switch OFF and leave the unit for about one hour, then load a disc and begin play.

■ Headphone operations

- Although the noise level is low, the volume level may be quite high during CD play. Do not raise the volume level of the headphones too excessively to avoid damaging ears.
- For traffic safety, do not use the headphones while driving a car.
- Be careful not to go to sleep while wearing the headphones.

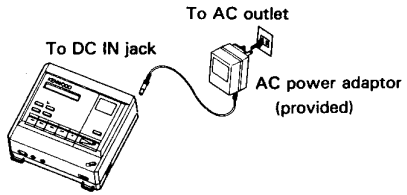
Power supply

After CD play, when about 30 seconds have elapsed in stop mode, the auto power-off function is activated, and the unit is automatically turned OFF to save power. To turn the power ON again, press the PLAY/PAUSE button, or any other button.
When the unit is not in use, be sure to place the POWER switch OFF. If you do not power will be consumed and battery life may be shortened.

■ When operating with the provided battery pack

- The battery pack provided is mounted for shipping. Before the unit can be operated with the battery pack for the first time after being unpacked, the battery pack must be charged for 8 hours.

How to charge the battery pack



Connect the provided AC adaptor to the player as shown in the figure on the left.
The time required for a full charge is about 8 hours.
When the player is operated while charging the battery pack, a slightly longer charging time will be required.

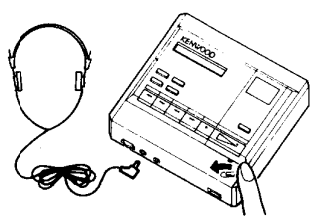
Notes:
- When charging the battery pack, be sure to use the provided AC adaptor. Using a battery pack other than the one provided may damage the player.
- To prevent leakage of the battery pack, do not place the battery pack standing up or on a slant while charging.
- Do not charge the battery pack in a place with poor ventilation, such as enclosed in a vinyl envelope.
- Be sure to charge the battery pack whenever it is exhausted.
- When the battery pack is not used for an extended period of time, charge it at least once every six months.
- If battery fluid leaks on the skin or clothes, immediately clean with running water.
- Do not place the battery pack into a fire.

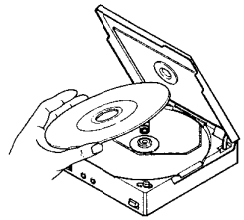
Operations (Normal play)

Before starting a play operation, be sure to set the VOLUME knob to "0". Since Compact Discs have a much lower noise level, if the volume level is set higher, the sudden output sound may damage your ears.

■ Preparations

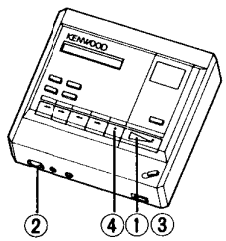
1 Connect headphones to the PHONES "1" or "2" jack.
2 Slide the OPEN switch to open the top cover.
3 Place a disc on the platter, with its label side up.





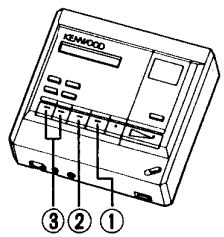
4 Close the top cover firmly, by pushing it until it clicks.
5 The disc starts rotating automatically, and about 3 and 4 seconds later, the total number of tunes contained on the disc (number of tracks) and their total playing time will be displayed in the display window.

■ To play continuously



① Press the PLAY/PAUSE button.
Play starts from the beginning of the disc.
② Raise the volume to an appropriate level with the VOLUME knob.
③ To stop play temporarily, press the PLAY/PAUSE button again. (At this time, the time display will blink.)
④ To stop play, press the STOP button.

■ Skip play and fast-forwarding/reversing



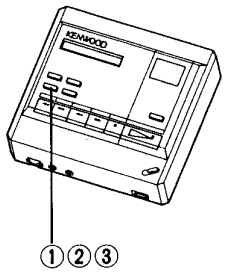
① Press the F-SKIP (▶▶|) button to quickly advance the playing position to the beginning of the next tune. Pressing the F-SKIP (▶▶|) button repeatedly will advance the playing position to the beginning of the tune ahead of the current tune by the number of times that the button is pressed.

② Press the R-SKIP (⏮) button to quickly return the playing position to the beginning of the current tune. Pressing the R-SKIP (⏮) button repeatedly will return the playing position to the beginning of the tune in back of the current tune by the number of times that the button is pressed.
- Even in stop mode, the playing position can be moved to the beginning of the desired tune (track) by pressing the F-SKIP (⏭) or R-SKIP (⏮) button.

③ During play, pressing the FF (▶▶) button will fast-forward the playing position, and pressing the REW (◀◀) button will fast-reverse the playing position.

■ To play repeatedly

- With the repeat function, whole tunes on the disc, only a desired tune (one track), or the programmed tunes (refer to the items in "Operations (Memory play)") can be played repeatedly.



① When the REPEAT button is pressed once, the "REPEAT one" display appears in the display window, and the currently playing tune will be played repeatedly.

② When the REPEAT button is pressed once more, the "REPEAT all" display appears, and all of the tunes on the disc will be played repeatedly. During memory play, all of the programmed tunes will be played repeatedly.

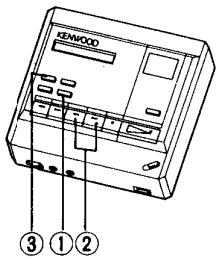
③ When the REPEAT button is pressed again, the "REPEAT" display goes off and the repeat function is disengaged.
- Repeat play can be activated even in stop mode.

Operations (Memory play)

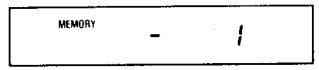
Memory play allows the tunes to be played in any desired order.

■ How to program tunes

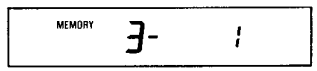
Programming tunes is possible only when the unit is in stop mode. First, press the STOP/M.CLEAR button to stop play.



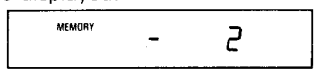
① Press the MEMORY/M.ALL CLEAR button. The "MEMORY" indicator lights up and the program number ("1" at first) will be displayed.



② Select the tune to be programmed by pressing the F-SKIP or R-SKIP button. (The following example shows that the 3rd tune is programmed.)



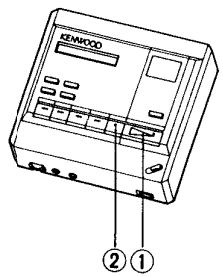
③ Press the REMAINING/M.ENTER button to program the tune. The next program number will be displayed.



④ Repeat procedures ② and ③ to program more tunes. Up to 16 tunes can be programmed for memory play.

- When you try to program more than 16 tunes, the first programmed tune (program number "1") will be replaced with the tune which is programmed in the 17th order.
- During programming, if you wait for an interval of more than about 30 seconds, the automatic power-off function is activated, and all programmed memories will be cleared. In this case, to program the tunes again, first press the MEMORY/M.ALL CLEAR button.

■ How to start memory play

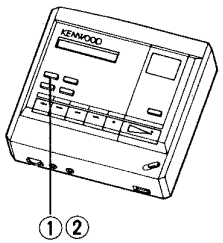


① Press the PLAY button.
- During memory play, skipping tunes, or fast-forwarding in the programmed order is possible using the F-SKIP (⏭), R-SKIP (⏮), FF (▶▶), or REW (◀◀) button.
- During memory play, single tune repeat, or all repeat, play is possible within the programmed tunes by pressing the REPEAT button.

② To stop memory play, press the STOP ■/M.CLEAR button.

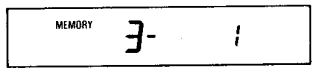
Note:
When the STOP ■/M.CLEAR button is pressed in stop mode, any programmed tunes will be sequentially cleared, in the order in which they were programmed.

■ To check the program content



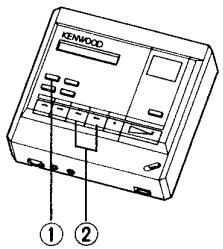
Set the player to stop mode.

① Press the REMAINING/M.ENTER button.
The first program number and the corresponding track number will be displayed.



② In this way, the memory contents will be displayed sequentially by pressing the REMAINING/M.ENTER button.
- When the program number next to the last programmed number is displayed, pressing the button again will display the first programmed contents.

■ To change the program content



Set the player to stop mode.

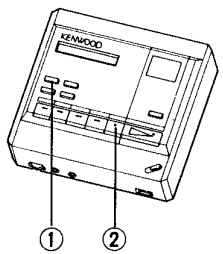
① Press the REMAINING/M.ENTER button repeatedly until the program number to be changed is displayed.

② Select the desired tune (track number) by pressing the F-SKIP (▶▶|) or R-SKIP (|◀◀) button.

③ Press the REMAINING/M.ENTER button to place the selected tune in memory.

④ To change another tune(s), repeat procedure ① and ② .

■ To delete part of the program



Set the player to stop mode.

① Press the REMAINING/M.ENTER button repeatedly until the tune (track number) to be deleted is displayed.

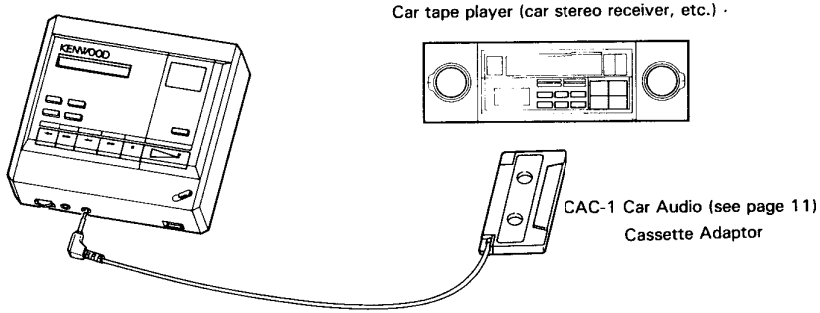
② Press the STOP ■/M.CLEAR button to delete the track number.
- At this time, the track number which was programmed as the next program number will be displayed.

■ To delete the entire program

Press the MEMORY/M.ALL CLEAR button and place the POWER switch to OFF ◄, or open the top (disc) cover. The entire programmed memory will be cleared.

To play in a car

This player has a car audio cassette adaptor for use in a car.
Along with these instructions, carefully read the provided CAC-1 Car Audio Cassette Adaptor instructions.

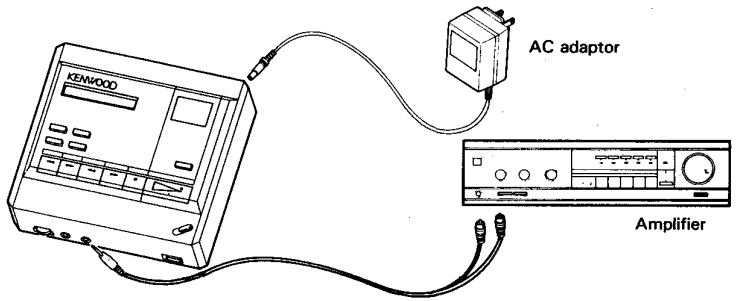


- For a power supply, use the provided battery pack.
  Be careful, as power cannot be supplied to the player directly from the car cigarette lighter socket.
- Connect the plug of the CAC-1 Car Audio Cassette Adaptor to the PHONES 2/LINE jack of the player.
- Insert the CAC-1 into the cassette slot of the car tape player.
- Set the cassette deck of the car tape player to play mode.

Notes:
- Depending on the car tape player the CAC-1 may not function.
- Do not leave the player in a car with the windows closed, to avoid subjecting it to high temperatures.
- Put the player in a place which is soft and is as free from car vibrations as possible.

To play with a home audio system

This player can be used with a home audio system in your listening room by connecting it to an amplifier. It can then be enjoyed with your loudspeaker system.



- Connect the provided AC adaptor for the power supply.
- Connect the connection cord provided to the PHONES 2/LINE jack of the player. Connect the white plug at the opposite end of the connection cord to the L (left) AUX IN jack and the red plug to the R (right) AUX IN jack respectively.
- When playing, set the VOLUME knob to the 7 position for an optimum output level.

Notes:
- Be sure to turn the amplifier's power off before making any connections.
- If the CD player interferes with radio or television broadcast reception, place the player away from the receiver or disconnect the power cord of the tuner or television set.

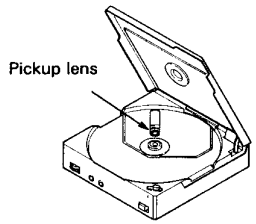
Simple maintenance

■ To clean the cabinet

To cleaning the cabinet of the player, wipe it with a dry soft cloth. When the cabinet is excessively dirty, use a cloth slightly dipped in water, and then wipe off with dry cloth.

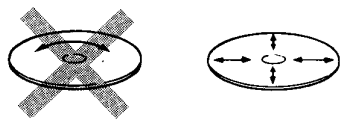
■ To clean the pickup lens

Use a commercially available blower for camera maintenance, etc., and blow the dust out of the lens.



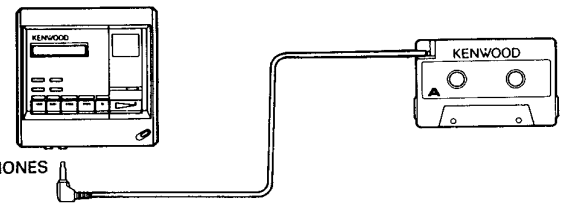
■ Disc handling

When the recorded surface of the compact disc is contaminated with fingerprints or dust, etc., wipe it off gently, using a commercially available cleaning cloth (exclusively for compact discs).
When cleaning, wipe in a radial direction, not in a circular direction.

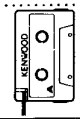
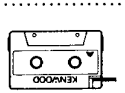
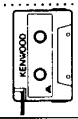


Operations

1. Lower the volume of both the CD player and the car stereo to avoid sudden excessively large sound output.
2. **Connections:**
   Insert the plug of the cord extending from the CAC-1 into the CD player.



3. The **CAC-1** inserting direction differs for each type of car stereo used, and depends on the cassette insertion slot of the cassette deck section. Refer to the following chart for loading instructions.

	Auto-reverse cassette deck			Normal (one-direction)
Cassette insertion slot (Car stereo)	⬆	⬆	⬆	⬆
CAC-1				
	Tape side to be played			Load with side A facing up
	For playback of upper side	For playback of lower side	For playback of upper side	
Notes		In this case, first replace the attached hooking prevention lug with the one provided.		
	If sound is not heard, or is very low, reverse the tape running direction to the opposite side.			

4. After placing the CAC-1 into the car stereo cassette insertion slot, raise the volume level of the car stereo to the normal listening position. Then adjust the volume of the CD player. (After this, use the car stereo control to adjust the volume level.)
5. To remove the CAC-1 from the car stereo, press the EJECT button in the same way as for cassette tapes.

Unusable Car Stereo Types

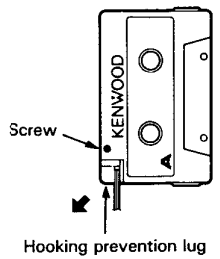
The CAC-1 cannot be used with the following types of car stereos.

a) One-direction cassette receivers in which the head is located on the left side.
b) Cassette receivers which function by detecting the tape tension. (In this case, when loading the CAC-1, it will be ejected.)
c) Car stereo models where the CAC-1 signal cord interfere with the insertion and removal of the CAC-1.

Replacement of Hooking Prevention Lug

To replace the attached hooking prevention lug, connected to the signal cord outlet of the CAC-1, with the one supplied, perform the following.

a) Loosen the screw located close to the cord outlet.
b) Remove the lug by pulling it in the direction of the arrow, as shown in the figure.
c) Insert the supplied lug by pushing it in the direction opposite to the arrow. (At this time, the lug is on side A.)
d) Tighten the screw.



The **CAC-1** is a Car Audio Cassette Adaptor which permits a portable CD player to be used in a car in combination with cassette car stereo equipment.

The **CAC-1** employs an electromagneticly coupled head, which does not directly contact the car stereo head, for higher fidelity sound.

Specifications

Frequency response	50 - 20,000 Hz (depending on the car stereo used)
Dimensions	102.4 x 12.1 x 63.8 mm
Weight	45 g
Cord length	1.5 m
Accessories	Hooking prevention lug x 1

CIRCUIT DESCRIPTION

DESCRIPTION OF COMPONENTS

Component	Use/Function	Operation/Condition/Compatibility
U101	RF amplifier	See the IC description. (p.13)
U301	Servo amplifier	See the IC description. (p.19)
U302	Operation amplifier	Amplifies the feed motor drive signal.
U351	Actuator control	See the IC description. (p.24)
U352	Motor control	See the IC description. (p.24)
U401	Digital signal processor	See the IC description. (p.25)
U402	Static RAM	See the IC description. (p.51)
U403	Microprocessor	See the IC description. (p.48)
U501	D/A converter	See the IC description. (p.52)
U502	Audio amplifier	Buffer amplifier for DAC output.
U503	LPF	Low-pass filter.
U801	4-input-NOR gate	Generates the reset signal.
U802	Operational amplifier	1/2 Vcc generator for the audio circuit.
U803	Regulated power supply	Limiter for the rechargeable battery.
Q101	LD switch	Switches the pickup's laser diode ON/OFF.
Q301	Tracking	Switches the ATSC circuit OFF during playback of a scratched disc (DEFECT-H).
Q302	Focusing signal switch	Holds the focusing offset position during playback of a scratched disc (DEFECT-H).
Q401	Power switch	Switches the power to the whole system, except for the CPU.
Q501	Emphasis	Applies emphasis when an emphasis signal is detected by the CPU.
Q502	Muting	Mutes the audio signal.
Q503	High filter	When the key is pressed, the CPU outputs an ON/OFF signal to switch the filter circuit ON/OFF.
Q504	Muting	Mutes the audio signal.
Q505	Muting driver	Controls Q502. Receives the muting signal from the microprocessor and switches the signal level ON/OFF.
Q506	Muting driver	When power is switched OFF, Q506 turns ON to drive Q502 and Q508.
Q507	Muting driver	When the supply voltage drops (3.5 V), Q507 turns OFF, turning the muting drivers ON.
Q508	Muting driver	Controls Q504 (same operation as Q502).
Q804	Actuator/motor drive power switch	Supplies power to the actuator and motor driver IC.
Q805, 806, 808	Ripple filter	Ripple filter for the audio circuit power supply.
Q807	Ripple filter switch	Switches the audio circuit power ON/OFF according to an ON/OFF signal from the CPU.
Q3001	Tracking brake	Brakes the tracking mechanism during playback of a scratched disc (DEFECT-H).
Q3002	Feed brake	When the inner feed limit switch turns ON, stops the feed mechanism from moving toward the inner tracks.

CIRCUIT DESCRIPTION

U101: RF AMPLIFIER FOR THE CD (CXA1081M)

Note: The following only describes the required features, as extracted from the Handbook.

General

The CXA1081M is an IC developed for use in Compact Disc players. It incorporates a 3-spot optical pickup RF output amplifier, a focusing error amplifier, a tracking error amplifier, and other signal processing circuitry, such as focus OK, mirror, defect, and EFM comparator circuits, as well as a laser diode APC (Automatic Power Control) circuit.

Features

- Operates on a signal +5 V power supply, as well as on a ±5 V dual-voltage power supply.
- Low power consumption (100 mW with ±5 V, 50 mW with +5 V).
- An APC circuit which accepts either a P-sub or N-sub laser diode.
- A minimum of external parts required.
- A disc defect detector circuit for improved playability.

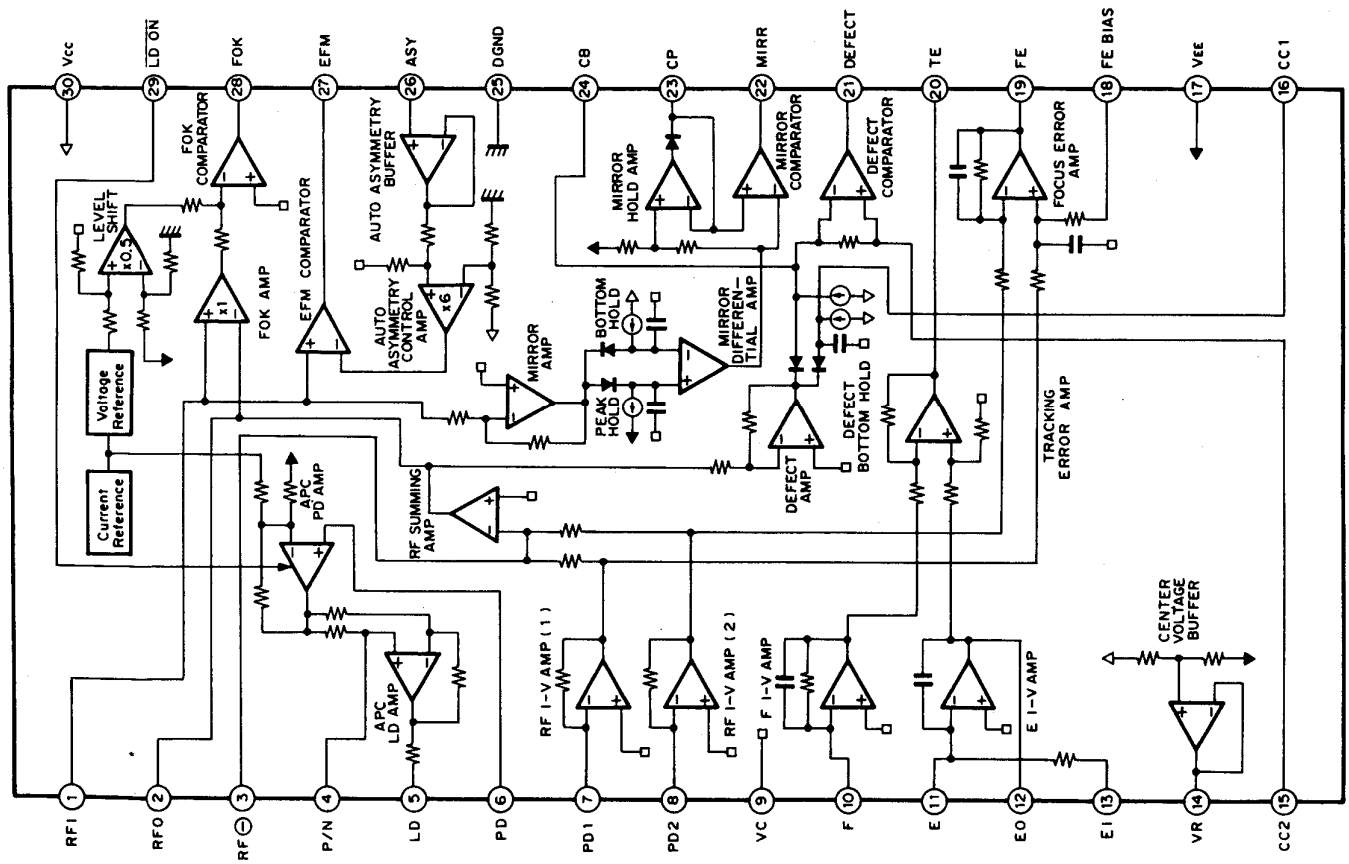
Structure

Bipolar silicon monolithic IC

Functions

- RF amplifier
- Focus OK detector circuit
- Mirror detector circuit
- Tracking error amplifier
- Defect detector circuit
- APC circuit
- EFM comparator
- Auto asymmetry control amplifier

Block diagram



CIRCUIT DESCRIPTION

Terminal explanation (V_{CC} = 2.5 V, V_{EE} = D_{GND} = −2.5 V, VC = GND)

Terminal No.	Terminal name	I/O	DC voltage (V)	Function
1	RFI	I	0	Input pin for the C-coupled signal output from the RF summing amplifier.
2	RFO	O	V_{RFO}	RF summing amplifier output pin. Used as the check point for the eye pattern.
3	RF⊖	I	0	RF summing amplifier feedback input pin.
4	P/N	I	0 (VC)	P-sub/N-sub select pin for the LD (Laser Diode). (DC voltage: in N-sub mode)
5	LD	O	−1.8	*APC LD amplifier output pin. (DC voltage: PD open in N-sub mode)
6	PD	I	0	*APC LD amplifier input pin. (DC voltage: open)
7	PD1	I	0	RF I-V amplifier (1) inverted input pin. Current input by connecting to the photodiode A+C terminal.
8	PD2	I	0	RF I-V amplifier (2) inverted input pin. Current input by connecting to the photodiode B+D terminal.
9	VC	—	0	Connected to GND when using a positive (+)/negative (−) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	0	F I-V amplifier inverted input pin. Current input by connecting to the photodiode F terminal.
11	E	I	0	E I-V amplifier inverted input pin. Current input by connecting to the photodiode E terminal.
12	EO	O	0	E I-V amplifier output pin.
13	EI	I	0	E I-V amplifier feedback input pin. For E I-V amplifier gain adjustment.
14	VR	O	V_{CVO}	DC voltage output pin of (V_{CC} + V_{EE})/2.
15	CC2	I	1.0	Input pin for the C-coupled signal output from the defect bottom hold.
16	CC1	O	1.2	Defect bottom hold output pin.
17	V_{EE}	—	−2.5	Connected to the negative power supply when using a positive (+)/negative (−) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FE BIAS	I	0	Bias pin on the focus error amplifier non-inverted side. For CMR adjustment of the focus error amplifier.
19	FE	O	V_{FEO}	Focus error amplifier output pin.
20	TE	O	V_{TEO}	Tracking error amplifier output pin.
21	DEFECT	O	V_{DFCTL}	Defect comparator output pin. (DC voltage: connected to a 10 k-ohm load).
22	MIRR	O	V_{MIRL}	Mirror comparator output pin. (DC voltage: connected to a 10 k-ohm load).
23	CP	I	−1.3	Mirror hold capacitor output pin. Mirror comparator non-inverted input.
24	CB	I	0	Defect bottom hold capacitor connect pin.
25	DGND	—	−2.5	Connected to GND when using a positive (+)/negative (−) dual-voltage power supply. Connected to GND (V_{EE}) when using a single-voltage power supply.
26	ASY	I	—	Auto asymmetry control input pin.
27	EFM	O	V_{EFMH}	EFM comparator output pin. (DC voltage: connected to a 10 k-ohm load).
28	FOK	O	V_{FOKL}	FOK comparator output pin. (DC voltage: connected to a 10 k-ohm load).
29	LD ON	I	−2.5 (DGND)	LD ON/OFF select pin. (DC voltage: when LD ON)
30	V_{CC}	—	2.5	Positive power supply.

*APC: Automatic Power Control

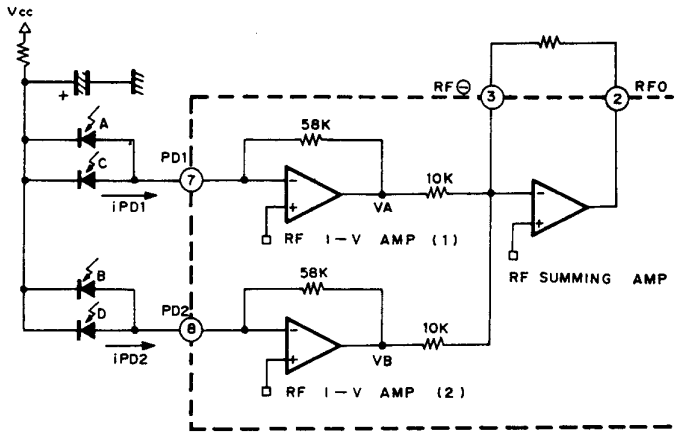
CIRCUIT DESCRIPTION

FUNCTION EXPLANATION

RF amplifier

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58 k-ohms in RF I-V amplifier (1) and (2) respectively.

The voltage which is converted from the current of the photodiode (A+B+C+D) is added in the RF summing amplifier and is output from the RFO pin. The eye pattern can be checked at this pin.



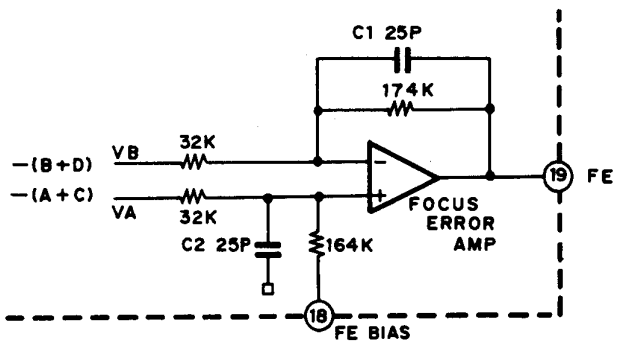
RF I-V AMPLIFIER

The low frequency component of the RFO output voltage, V_{RFO}, is represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6 \text{ k-ohms} \times (i_{PD1} + i_{PD2})$$

Focus error amplifier

The difference between the RF I-V amplifier (1) output (VA) and the RF I-V amplifier (2) output (VB) is calculated, and the current of the photodiode (A+C−B−D) is converted to a voltage and output.



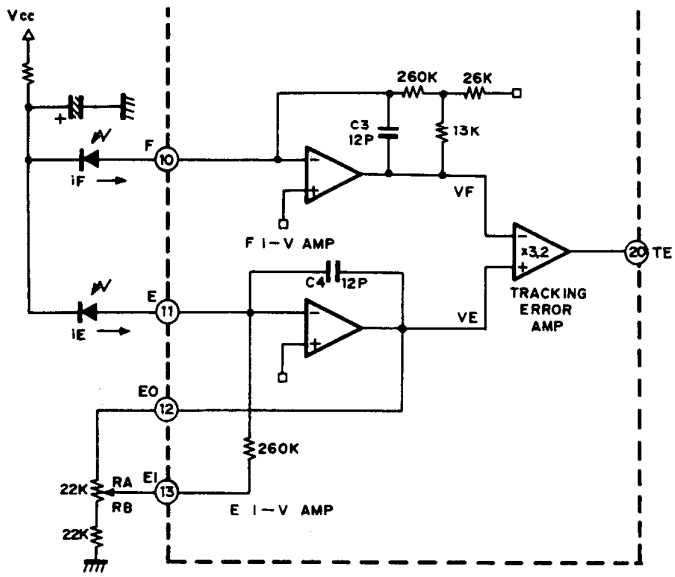
The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315.4 \text{ k-ohms}$$

The common mode rejection ratio of the VR connected to pin ⑱ is maximized when the composite impedance to GND is around 10 k-ohms (with a VR resistance of around 40 k-ohms).

CIRCUIT DESCRIPTION

Tracking error amplifier



The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I-V amplifier and F I-V amplifier respectively.
That is:

$V_F = iF \times 403$ k-ohms

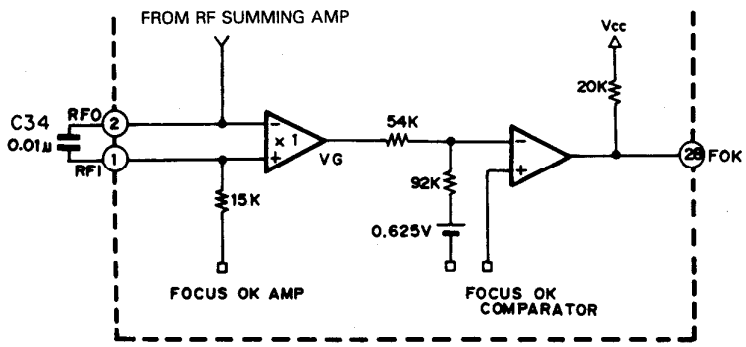
$V_E = iE \times 260$ k-ohms $\times R_A/(R_B + 22\ k) + (R_A + 260\ k)$

The difference between the E I-V amplifier and the F I-V amplifier is calculated by the tracking error amplifier, and the photodiode (E-F) current is converted to a voltage and output.

$V_{TE} = (V_E - V_F) \times 3.2$

$= (iE - iF) \times 1290$ k-ohms

Focus OK circuit



The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.
While an RF signal is present at pin ②, an HPF output is present at pin ①. At the same time, the LPF output (opposite phase) of the focus OK amplifier is obtained.
The focus OK output is inverted when $V_{RFI} - V_{RFO}$ is almost equal to −0.37 V.

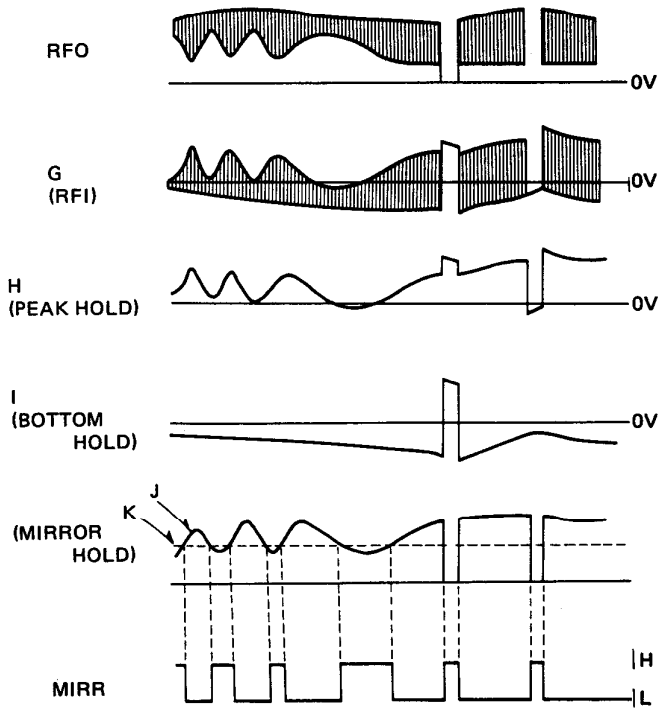
C34 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amplifier. Normally, C34 = 0.01 μF is selected, with fc = 1 kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.

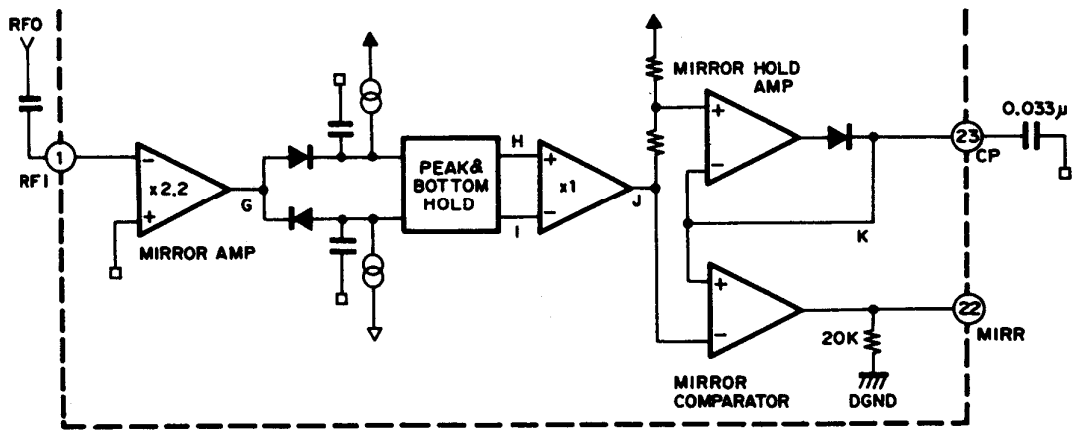
CIRCUIT DESCRIPTION

Mirror circuit

In the mirror circuit, after the RFI signal is amplified, both its peak and bottom are held.

While the peak hold is held by a time constant which can follow a traverse of 30 kHz, the bottom hold is held by a time constant which can follow a cyclic period envelope variation.



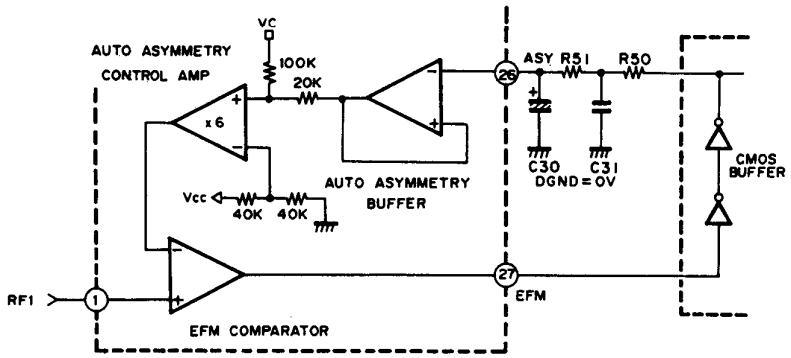


These peak and bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J. This signal is compared with signal K, which is obtained by a peak hold with a large time constant corresponding to 2/3 of the peak value, so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite large when compared with the traverse signal.

CIRCUIT DESCRIPTION

EFM comparator

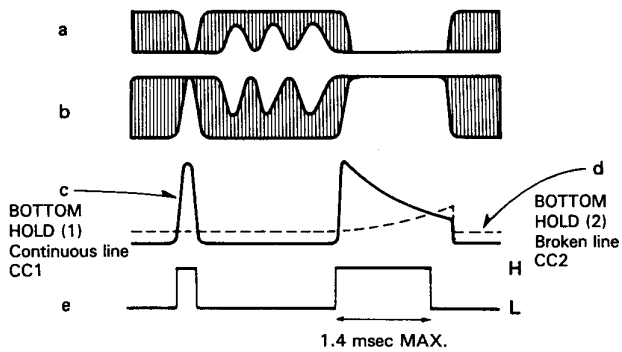
The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristic that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal.

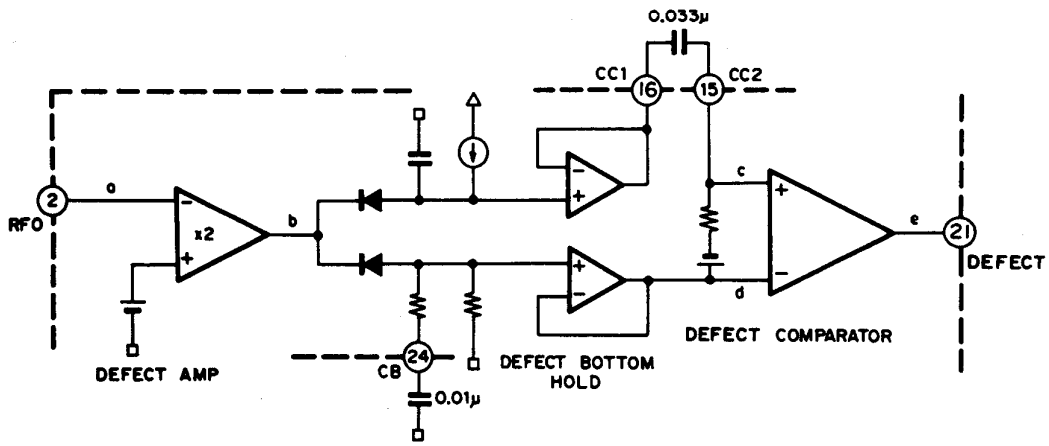


The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer. R8, R9, C8 and C9 constitute an LPF to obtain the DC component of (Vcc+DGND)/2 (V). If the cut-off frequency (fc) is set to more than 500 Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.

Defect circuit

After inverting the RFI signal, the defect circuit bottom holds with two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1 msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generate the mirror defect detecting signals.





CIRCUIT DESCRIPTION

U301: SERVO SIGNAL PROCESSOR FOR THE CD (CXA1082Q)

General

The CXA1082Q is a bipolar IC developed for servo control in Compact Disc players.

Features

- Operates on a signal +5 V power supply as well as on a ±5 V dual-voltage power supply.
- Low power consumption (165 mW with ±5 V, 100 mW with +5 V).
- Same servo function as CX20108 (focusing, tracking, sled servo)
- Built-in auto sequencer.
- Built-in spindle servo LPF.
- Built-in loop filter and VCO for an EFM clock generating PLL.
- A minimum of external parts required.
- Sled overrun prevention circuit.
- Disc defect treatment circuit.
- Anti-shock circuit
- Linear motor feed for high-speed access.
- Shared use of a serial data bus with the CX23035 and CXD1135Q.
- The microprocessor and software both have upward compatibility with the CX20108.
- The pulse height of the focusing search, track jump, and sled kick can be set with externally connected resistors.

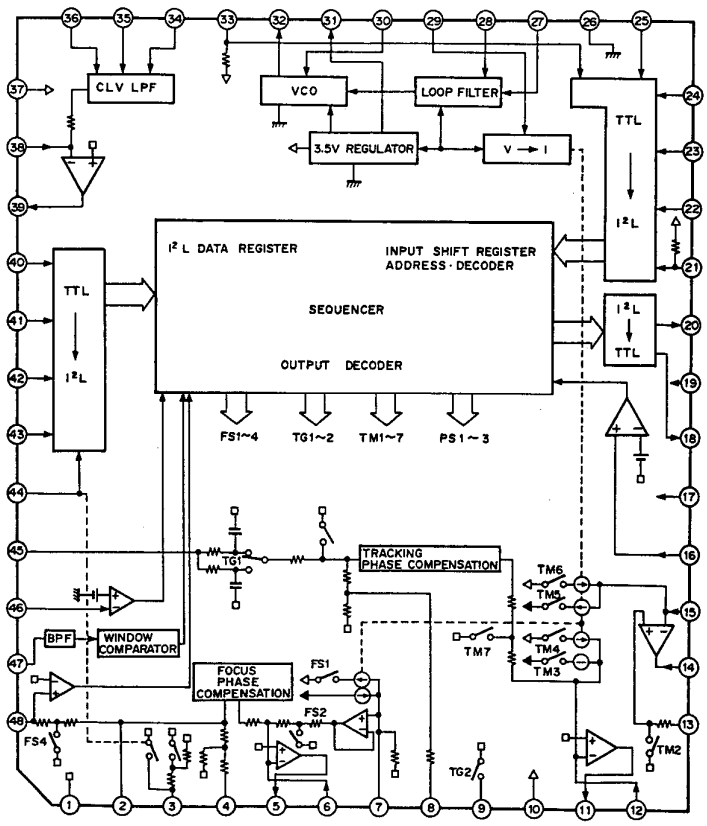
Functions

- Focusing servo control
- Tracking servo control
- Sled servo control
- Spindle servo
  Low Pass Filter, drive amplifier
- EFM clock generating PLL
  Loop filter: 8.64 MHz VCO
- Auto sequencer
  Incorporating a RAM

Structure

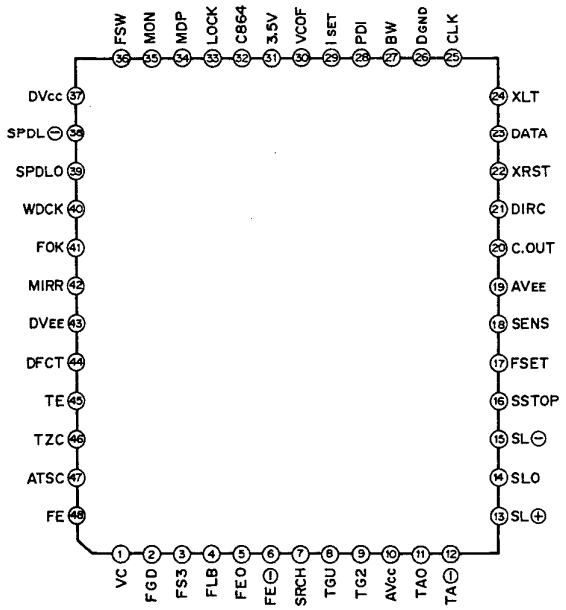
Bipolar silicon monolithic IC

Block diagram



CIRCUIT DESCRIPTION

Pin configuration

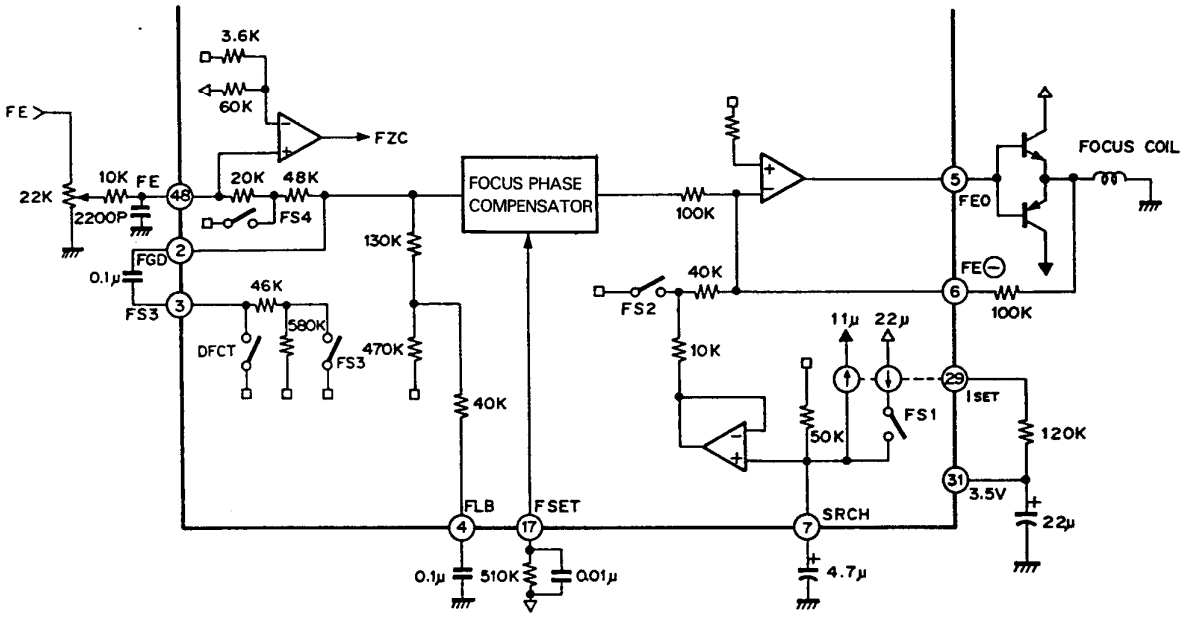


Terminal explanations

Terminal No.	Terminal name	Function
2	FGD	To lower the high frequency gain of the focus servo, insert a capacitor between this pin and pin 3.
3	FS3	The high frequency gain of the focus servo is selected by switching FS3 ON/OFF.
4	FLB	Time constant external connect pin, for boosting the focus servo low frequencies.
5 11 14 39	FEO TAO SLO SPDLO	Power transistor drive op amplifier output pins.
6	FE⊖	Focus amplifier inverted input pin.
7	SRCH	Time constant external connect pin, for creating the focus search waveform.
8	TGU	Time constant external connect pin, for selecting the tracking high frequency gain.
9	TG2	Time constant external connect pin, for selecting the tracking high frequency gain.
12	TA⊖	Tracking amplifier inverted input pin.
13	SL⊕	Sled amplifier non-inverted input pin.
15	SL⊖	Sled amplifier inverted input pin.
16	SSTOP	Limit switch ON/OFF detection signal input pin, for detecting the innermost edge of the disc.
17	FSET	Setting pin for the focus tracking phase peak value compensation, and fo of the CLV LPF.
18 20	SENS C.OUT	Output pins for an interface with a microprocessor.
21 22 23 24 25 33	DIRCT XRST DATA XLT CLK LOCK	Input pins for an interface with a microprocessor. A 47-kohm pull-up resistor is only incorporated in pins 21 and 33.
27	BW	Loop filter time constant external connect pin.
28	PDI	Input pin for the phase comparator output PDO of CXD23035/CXD1135.
29	ISET	Inputs a current which determines the level of the focus search, track jump, and sled kick.
30	VCOF	The self-advancing frequency of the VCO is almost proportional to the resistance between this pin and pin 31.
32	C864	8.64 MHz VCO output pin.
34	MDP	CXD23035/CXD1135 MDP pin connect pin.
35	MON	CXD23035/CXD1135 MON pin connect pin.
36	FSW	LPF time constant external connect pin, for the CLV servo error signal.
38	SPDL⊖	Spindle drive amplifier inverted input pin.
40 41 42 44	WDCK FOK MIRR DFCT	Input pins for an interface with a microprocessor.
45	TE	Tracking error signal input pin.
46	TZC	Tracking zero-cross comparator input pin.
47	ATSC	Window comparator input pin for ATSC detection.
48	FE	Focusing error signal input pin.

CIRCUIT DESCRIPTION

Focusing servo system



This block diagram is of the focusing servo system.

When FS3 is ON, the capacitor connected between pins 2 and 3 and the internal resistance determines the low-frequency time constant which can attenuate the high-frequency gain.

The capacitor between pin 4 and GND determines the time constant for boosting the low frequencies in normal playback.

The peak frequency of the focusing phase compensation is inversely proportional to the resistance connected to pin 17, and the frequency is about 1.2 kHz when the resistance is 510 k-ohms.

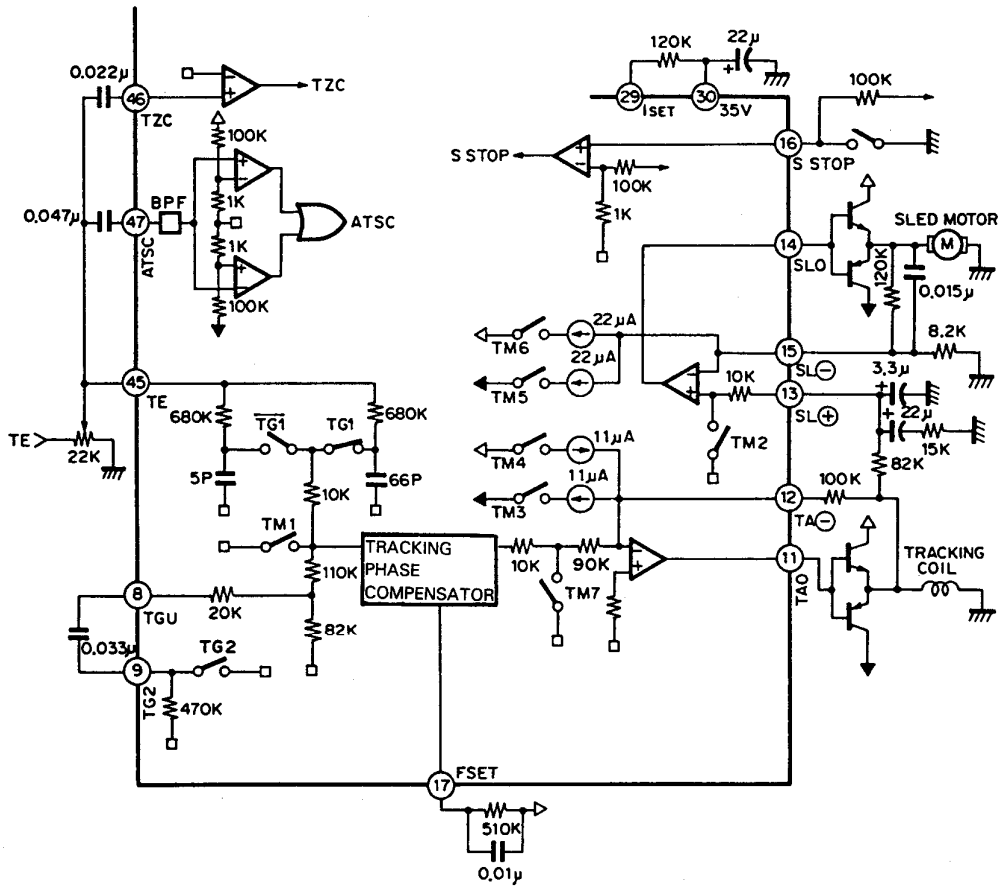
The focus search level is about ±1.1 Vp-p with these constants. The level is inversely proportional to the value of the resistance connected between pins 29 and 30. Note that the track jump and sled kick levels are also varied by changing this resistance.

The level has been set to 5.7% of the difference between Vcc, the inverted input reference voltage of the FZC comparator, and VC (pin 1); i.e. (Vcc−VC)×5.7%.

* Varying the value of resistance connected to pin 17 also varies the phase compensation peak values of focusing/tracking/sled servos and fc of the CVL LPF. At the same time, the op amplifier's dynamic range and offset voltage are also varied.

CIRCUIT DESCRIPTION

Tracking and sled servo system



This block diagram is of the tracking and sled servo system. The capacitor connected between pins 8 and 9 determines the time constant for attenuating the high-frequency gain. The peak frequency for the tracking phase compensation is inversely proportional to the resistance connected to pin 17, and the frequency is about 1.2 kHz when the resistance is 510 k-ohms.

A FWD or REV tracking jump is performed by switching TM3 or TM4 ON. At this time, the peak voltage applied to the tracking coil depends on the current at TM3 or TM4 and the feedback resistance through pin 12, as shown by the following equation:

Track jump peak voltage = TM3 (TM4) current × Feedback resistance

A FWD or REV sled kick is performed by switching TM5 or TM6 ON. At this time, the peak voltage applied to the sled motor depends on the current at TM5 or TM6 and the feedback resistance through pin 15, as shown by the following equation.

Sled jump peak voltage = TM5 (TM6) current × Feedback resistance

The currents at these switches are determined by the resistance connected between pins 29 and 31. When the value is 120 k-ohms, the currents are:

±11 μA at TM3 and TM4, and

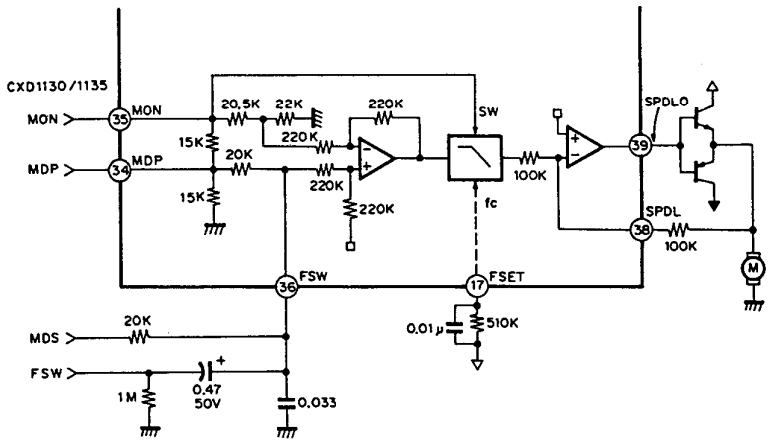
±22 μA at TM5 and TM6.

The currents are inversely proportional to the resistance, and the variable range is from about 5 to 40 μA with TM3.

S STOP is the signal used to detect the ON/OFF of the limit switch for detecting the innermost position for the linear motor.

CIRCUIT DESCRIPTION

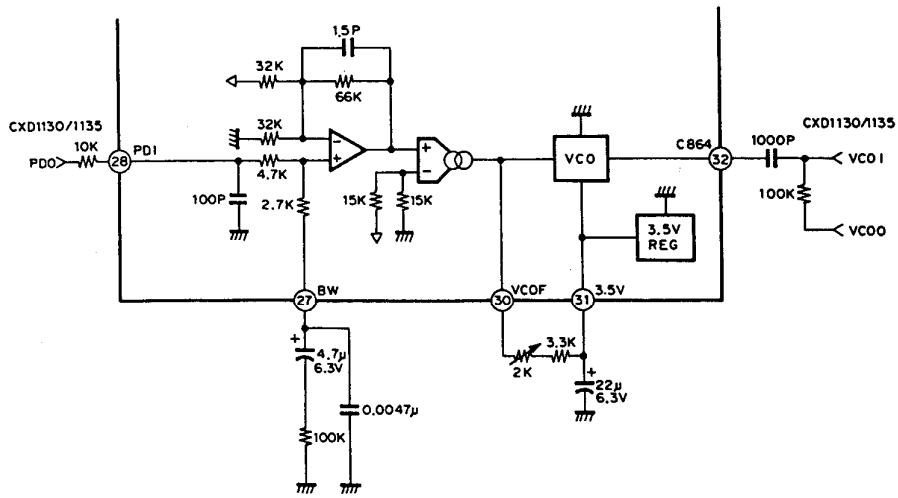
Spindle servo and LPF circuitry



The carrier component in the CLV servo error signals MDS and MDP are eliminated by a two-stage LPF, which consists of a 200 Hz LPF formed by a 0.033 μF capacitor and a 20 k-ohms resistor connected to pin 36 and an internal LPF (fc up to 200 Hz when 510 k-ohms is connected to pin 17).

In the CLV-S mode, FSW becomes L, and fc of the LPF at pin 36 drops to enhance the filtering effect. The resistor connected to pin 17 need not be stabilized but only connected to Vcc, because its fc will not be varied by supply voltage variation.

VCO loop filter and 8.64 MHz VCO circuitry



The phase comparator output, PDO, is input via pin 28, sent through the loop filter to eliminate the PWM carrier component, then V-I converted, and added with the self-advancing frequency set current from pin 30 for use in controlling the VCO frequency. The VCO's self-advancing frequency is almost proportional to the resistance connected between pins 30 and 31. The value of this resistance is set so that the PLL capture range center is 4.3218 MHz at CXD1135/1130 pin 70. The external circuit connected to pin 27 BW is used to maximize the capture range during accessing, so that access is possible even when the self-advancing frequency deviates due to the VCO's temperature characteristic, etc.

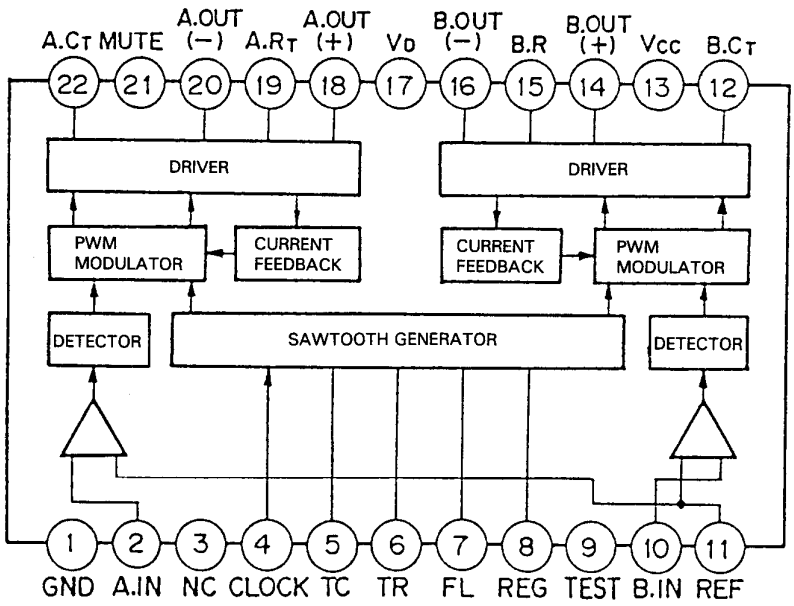
CIRCUIT DESCRIPTION

U351, U352: PWM DRIVERS FOR THE CD (CXA1083M)

Structure

Bipolar silicon monolithic IC

Block diagram



CIRCUIT DESCRIPTION

U401: DIGITAL SIGNAL PROCESSING LSI FOR THE CD (CXD1130Q)

General

The CXD1130Q is a digital signal processing LSI for a Compact Disc player, and has the following functions.

1. Bit clock reproduction by an EFM-PLL circuit
2. EFM data demodulation
3. Frame sync signal detection, protection and insertion
4. Powerful error detection and correction
5. Interpolation with an average value, or by holding the previous value
6. Demodulation of a sub code signal, error detection of a sub code Q
7. Spindle motor CLV servo
8. 8-bit tracking counter
9. CPU interface with a serial bus
10. Sub code Q register
11. Digital filter

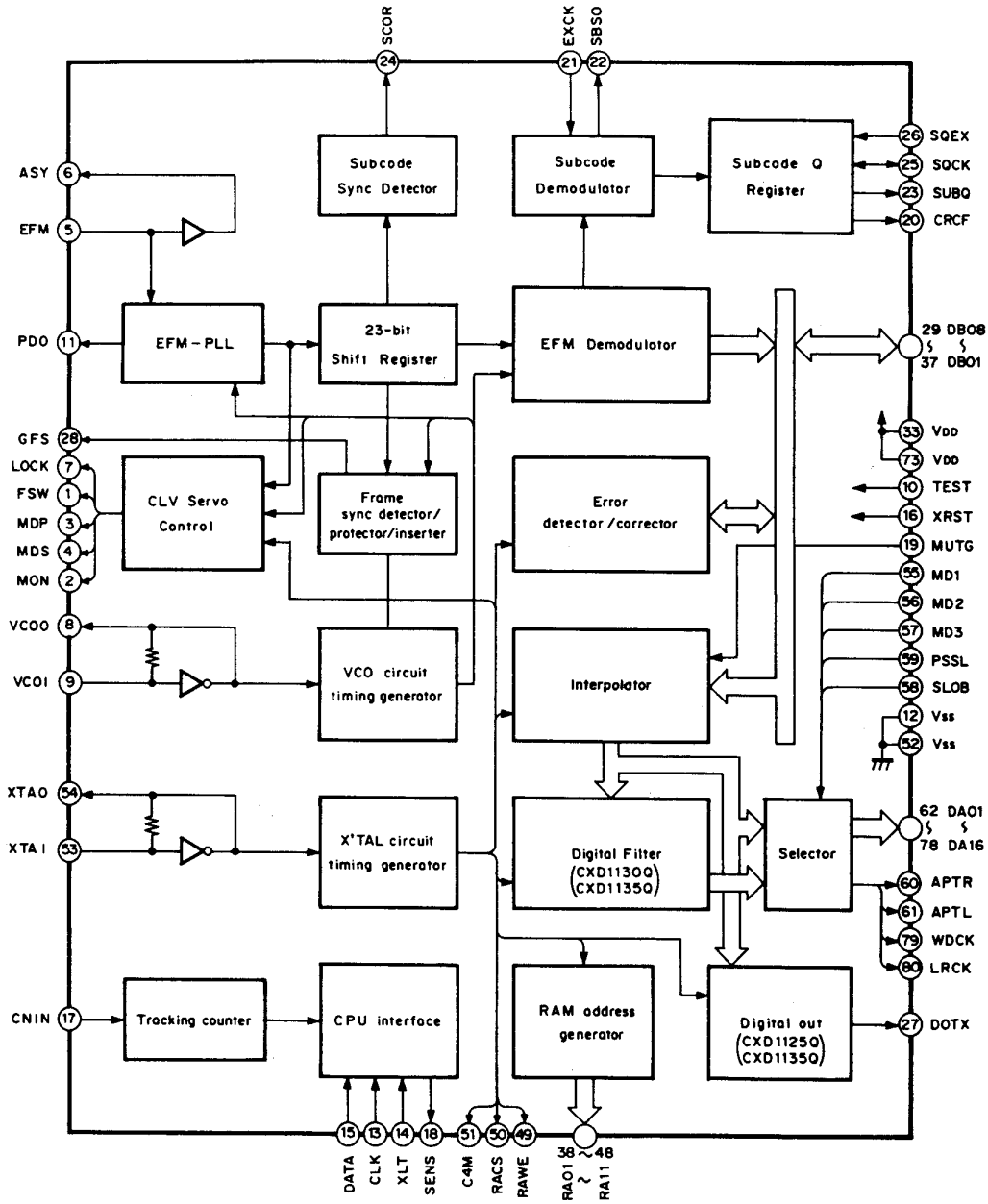
Features

- All digital signals used in playback can be processed using only a single chip.
- An aperture-correction digital filter is built in.

Structure

CMOS IC

Block diagram



CIRCUIT DESCRIPTION

Terminal explanations

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arrow, outputs "L".
8	VCOO	O	VCO output. f=8.6436 MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0 V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	V_{SS}	—	GND (0 V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENS	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case when ATTM of internal register A is "L". Normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code serial output.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync S0+S1 output.
25	SQCK	I/O	Sub code Q read-off clock.
26	SQEX	I	SQCK select input.
27	DOTX	O	DIGITAL OUT output. (Outputs the $\overline{\text{WFCK}}$ signal when CXD1130Q or D0 is off)
28	GFS	O	Display output of frame sync lock status.
29	DB08	I/O	Data pin of external RAM. DATA8 (MSB)
30	DB07	I/O	Data pin of external RAM. DATA7
31	DB06	I/O	Data pin of external RAM. DATA6
32	DB05	I/O	Data pin of external RAM. DATA5
33	V_{DD}	—	Power supply (+5 V)
34	DB04	I/O	Data pin of external RAM. DATA4
35	DB03	I/O	Data pin of external RAM. DATA3
36	DB02	I/O	Data pin of external RAM. DATA2
37	DB01	I/O	Data pin of external RAM. DATA1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (Active at "L").
50	RACS	O	Chip select signal output to external RAM. (Active at "L").
51	C4M	O	Crystal dividing output. f= 4.2336 MHz.
52	V_{SS}	—	GND (0 V).
53	XTAI	I	Crystal oscillator input. f=8.4672 MHz or 16.9344 MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f=8.4672 MHz or 16.9344 MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select input. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL="H", C1F1 output when PSSL="L".
63	DA02	O	DA02 output when PSSL="H", C1F2 output when PSSL="L".
64	DA03	O	DA03 output when PSSL="H", C2F1 output when PSSL="L".
65	DA04	O	DA04 output when PSSL="H", C2F2 output when PSSL="L".
66	DA05	O	DA05 output when PSSL="H", C2FL output when PSSL="L".
67	DA06	O	DA06 output when PSSL="H", C2PO output when PSSL="L".
68	DA07	O	DA07 output when PSSL="H", RFCK output when PSSL="L".
69	DA08	O	DA08 output when PSSL="H", WFCK output when PSSL="L".
70	DA09	O	DA09 output when PSSL="H", $\overline{\text{PLCK}}$ output when PSSL="L".
71	DA10	O	DA10 output when PSSL="H", UGFS output when PSSL="L".
72	DA11	O	DA11 output when PSSL="H", GTOP output when PSSL="L".
73	V_{DD}	—	Power supply (+5 V).
74	DA12	O	DA12 output when PSSL="H", RAOV output when PSSL="L".
75	DA13	O	DA13 output when PSSL="H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL="H", $\overline{\text{C21O}}$ output when PSSL="L".
77	DA15	O	DA15 output when PSSL="H", C21O output when PSSL="L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL="H", DATA output when PSSL="L".
79	WDCK	O	Strobe signal output. 176.4 kHz when DF is ON, 88.2 kHz with CXD1125Q or when DF is OFF.
80	LRCK	O	Strobe signal output. 88.2 kHz when DF is ON, 44.1 kHz with CXD1125Q or when DF is OFF.

Notes:

C1F1 :
C1F2 :] Error correction status monitor output for C1 decode.

C2F1 :
C2F2 :] Error correction status monitor output for C2 decode.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

C2PO : C2 pointer signal. Synchronized to the audio data output.

RFCK : Read frame clock output. 7.35 MHz when locked to the crystal line.

WFCK: Write frame clock output. 7.35 MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f=4.3218 MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. 352.8 kHz when DF is ON, 176.4 kHz with CXD1125Q or when DF is OFF.

$\overline{\text{C21O}}$: C21O invert output.

C21O : Bit clock output. 4.2336 MHz when DF is ON, 2.1168 MHz with CXD1125Q or when DF is OFF.

DATA : Audio signal serial data output.

CIRCUIT DESCRIPTION

Explanation of functions

1. CPU interface

(1) Data input

Each register may be set by input of 4-bit address, and 4-bit data from LSB in the timing that is shown in Fig. 1 to three pins, XLT, CLK and DATA. The address and data of each pin are as shown in Table 1, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".

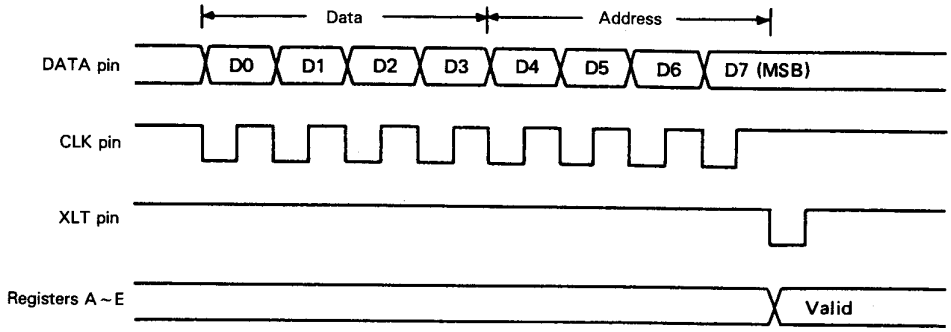


Fig. 1 Timing chart for data input

(2) Registers

Register 9 — New function control

Controls the new functions address to the CX23035.

D0 : CRCQ — Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in "**1-(5). Subcode output**". (Page 31)

D1 : NCLV — Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in "**6. CLV servo control**". (Page 37)

D2 : HZPD — One of the defect countermeasures. Switches ON/OFF the function which makes the PDO pin a high impedance (Z) for a maximum of 0.55 ms from the trailing edge of GFS. Details are described in "**10. Countermeasures to defects**". (Page 44)

D3 : ZCMT — Switches the zero cross mute function ON/OFF. Details are described in "**7. Interpolation and mute, attenuate**". (Page 42)

Register A — Sync. protection, attenuator control

D0 : ATTM — Used for attenuating audio signals by 12 dB.

D1 : WSEL, D2 : GSEL, D3 : GSEM — Provided for switching frame sync. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of "**2. EFM demodulation**". (Page 33)

Registers B and C — Counter set, more significant 4-bit (register C) and less significant 4-bit (register B)

These registers are used for setting the tracking counter value. The data of registers B and C are preset in the counter through the 4-bit buffer register assigned by address. Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8-bit data (either buffer register is of "OLD" data).

Register D-CLV control

D0 : GAIN — Used for setting the gain of MDP pin output in the CLV-S and CLV-H modes. It is −12 dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0 dB when D0 = 1.

D1 : T_P — Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D2 : T_B — Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK/32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D3 : DIV — Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0, phase comparison of RFCK/4 and WFCK/4 is made, and output is made out of MDP pin in each case.

CIRCUIT DESCRIPTION

Register E – CLV mode

It is as shown in Table 1.

The details of each mode will be described in "**6. CLV servo control**". (Page 37)

D3 to D0 are all "0" when XRST = L.

Register name	Command	Address D7 ~ D4	Data				SENS pin
			D3	D2	D1	D0	
9*1	New function control	1001	ZCMT	HZPD	NCLV	CRCO	Z
A*2	Sync protection attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4-bit	1011	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4-bit	1100	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*3	CLV control	1101	DIV	T_B	T_P	GAIN	Z
E*4	CLV mode	1110	CLV mode				$\overline{\text{PW} \geqq 64}$

***1 Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDO pin is always active.	PDO pin is "Z" at the trailing edge of GFS.
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

***2 Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG pin	dB
0	0	0
0	1	$-\infty$
1	0	−12
1	1	−12

***3 Register D**

DIV	D3	0	RFCK/4, WFCK/4
		1	RFCK/8, WFCK/8
T_B	D2	0	RFCK/32
		1	RFCK/16
T_P	D1	0	RFCK/4
		1	RFCK/2
GAIN	D0	0	−12 dB
		1	0 dB

DIV	Phase comparison frequency in CLV-P mode
T_B	Bottom hold period in CLV-S, CLV-H mode
T_P	Peak hold frequency in CLV-S mode
GAIN	Gain at MDP pin in CLV-S, CLV-H mode

***4 Register E**

Mode	D3 ~ D0	MDP pin	MDS pin	FSW pin	MON pin
STOP	0000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	CLV-P	Z	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z: High impedance

Table 1 List of registers

CIRCUIT DESCRIPTION

(3) Tracking counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in registers B and C. Count of CNIN pulses is started at rising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal (COMPLETE) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENS pin. When the address is set at "C", signal (COUNT) of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig. 2.

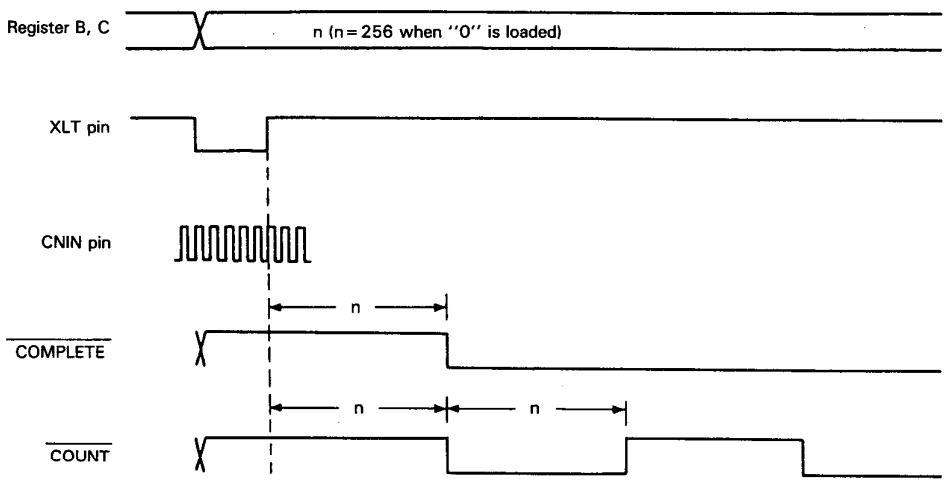


Fig. 2 Tracking counter timing chart

(4) SENS

The following signals are output from SENS pin depending on the address of D7 ~ D4.

(1) COMPLETE : Address (see note) is "B"; Shown in Fig. 2.

(2) COUNT : Address (see note) is "C"; Shown in Fig. 2.

(3) PW≧64 : Address (see note) is "E"; This signal is of LOW level when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note: Address setting is determined by the data corresponding to D4 to D7, which are input from the DATA pins shown in Fig. 1.

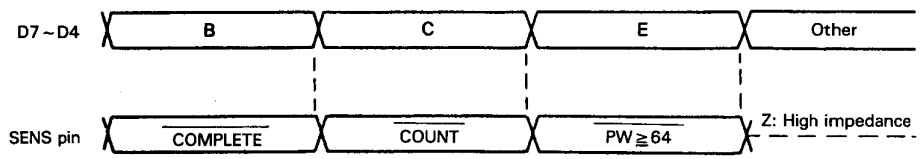


Fig. 3 Timing chart of SENS pin

CIRCUIT DESCRIPTION

(5) Sub code output

Sub codes P~W loaded in the 8-bit shift register are output out of SBSO pin in accordance with the clock input through EXCK pin. When SCOR pin is "H", S0+S1 signal is output. Sub code Q is as follows, depending on the SQEX pin status.

a. When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The WFCK is also output from the SQCK pin.

b. When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated as shown in Fig. 7, and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF="H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4-bit, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4-bit of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF

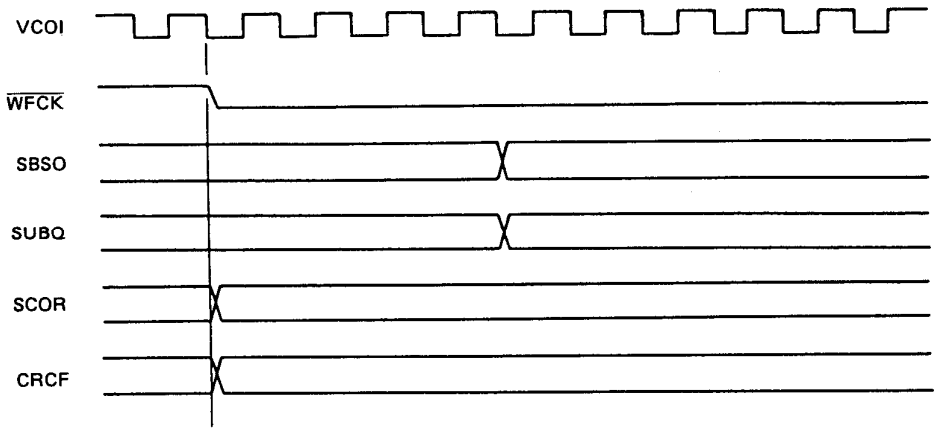
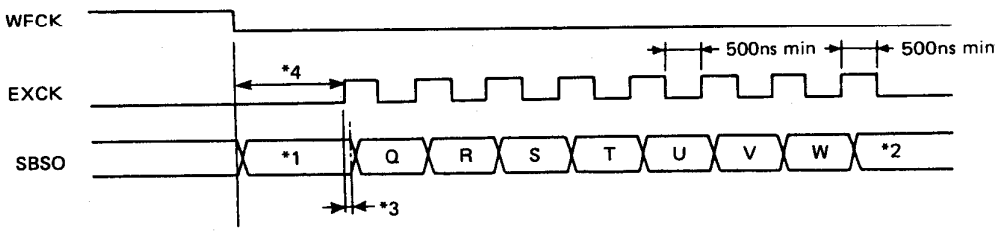


Fig. 4

(b) Timing of SBSO, EXCK



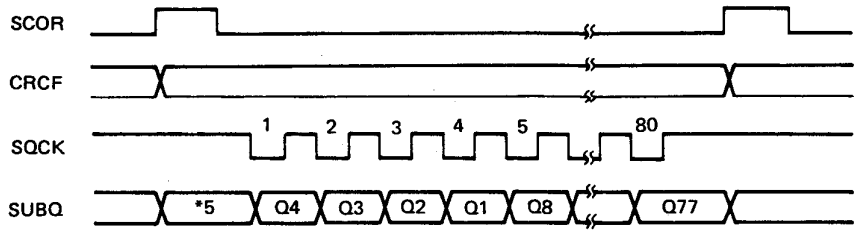
*1: Sub code P is output when SCOR is 0.
S0+S1 is output when SCOR is 1.
*2: SBSO is 0 when 8 or more pulses are input to EXCK.
*3: 4T~6T if the period of VCO is expressed as T.
*4: Make EXCK low for 10 μs from the rising edge of WFCK.
One time period of T=8.6436 MHz.

Fig. 5 Timing chart of sub code outputs

CIRCUIT DESCRIPTION

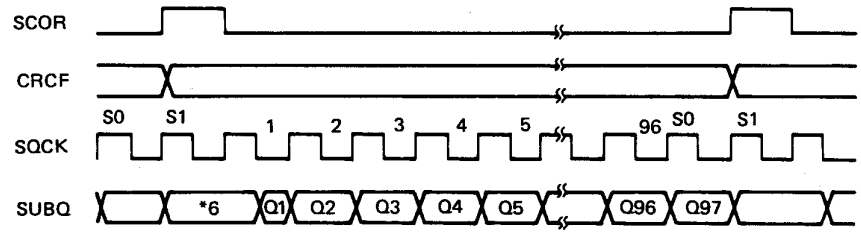
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX = "H" level



*5:CRCF when CRCQ flag is "1", undefined when "0".

SQEX = "L" level



*6:CRCF when CRCQ flag is "1", Q98, Q1 when "0".

Fig. 6 Timing chart of sub code outputs

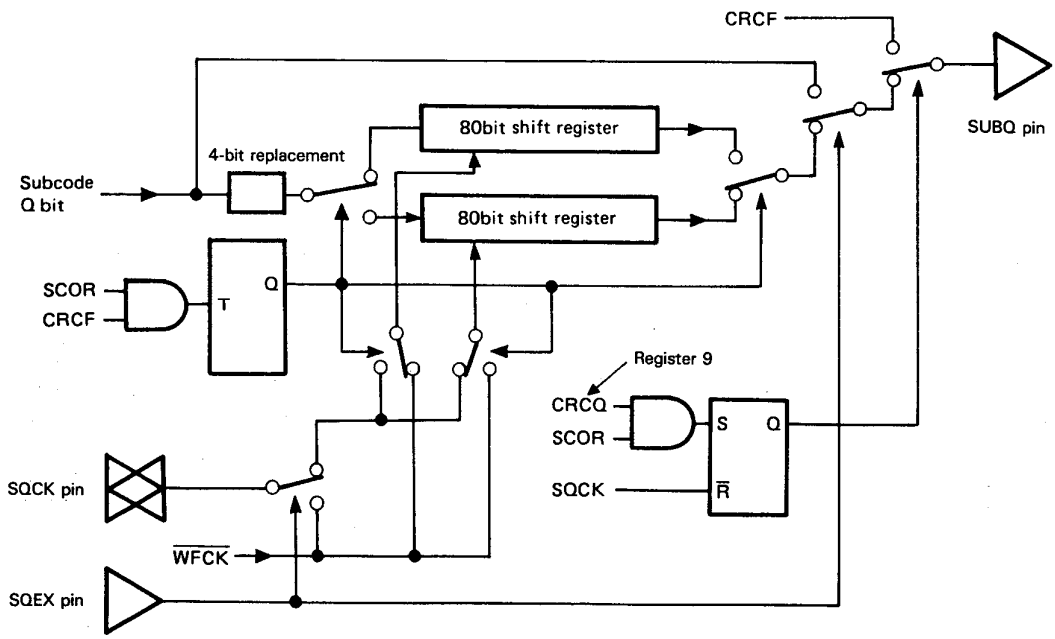


Fig. 7

CIRCUIT DESCRIPTION

2. EFM demodulation

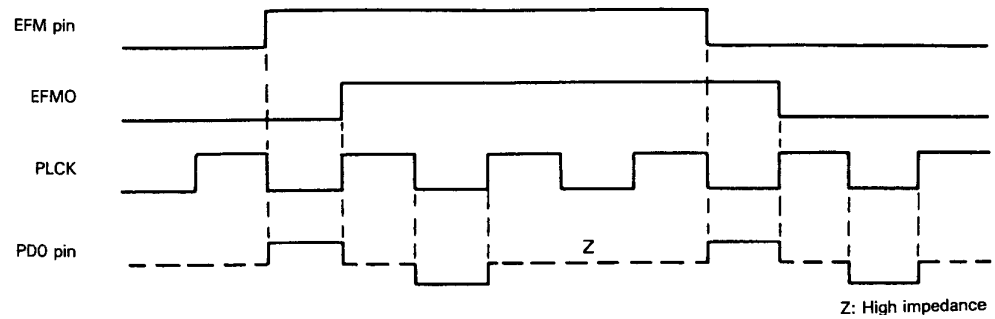
(1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16 MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32 MHz synchronized with this clock by the EFM-PLL circuit.

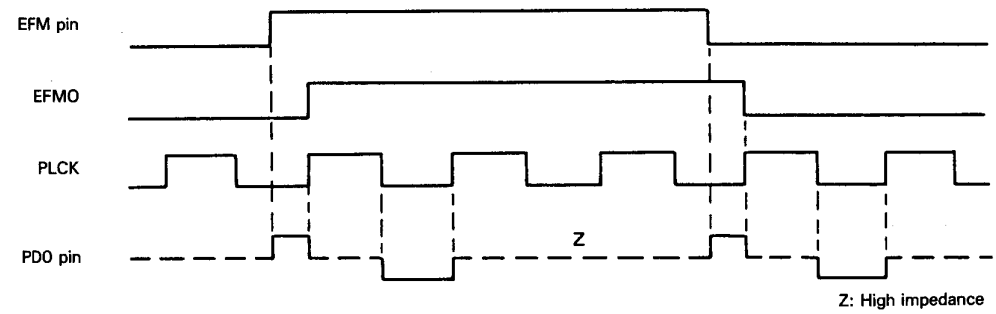
At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO pin. The mean value of PDO pin is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

The timing charts of EFM pin, EFMO, PLCK and PDO are shown in Fig. 8.

(a) When EFM signal and VCO are synchronized



(b) When VCO is higher than EFM signal



(c) When VCO is less than EFM signal

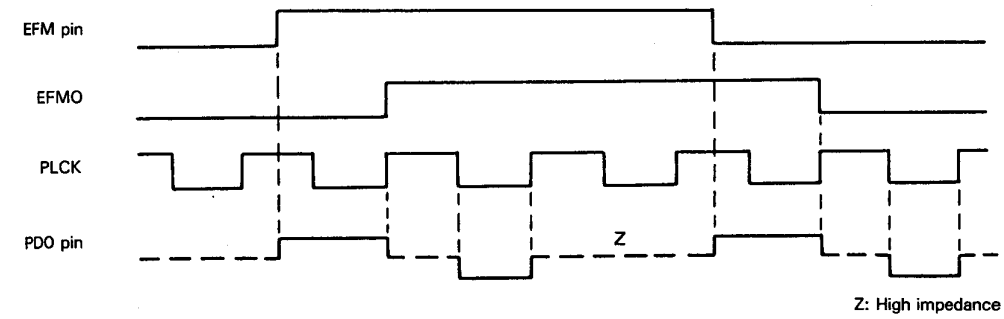


Fig. 8 Timing charts of EFM-PLL circuit

CIRCUIT DESCRIPTION

(2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23-bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL.

If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218 MHz/588 = 7.35 kHz)

A 4-bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4-bit counter is reset with the next frame synchronizing signal. The GTOP pin is of "H" while this operation is performed. Further, GSF pin is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the window is output out of UGFS (DA05 pin at the time when PSSL = L).

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frame to be interpolated	UGFS (PSSL = L)
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ). Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

(3) EFM demodulation

14-bit data is taken out of the 23-bit shift register and is demodulated to 8-bit data through 14 →8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08 - DB01 pins) of the RAM in accordance with the OENB signal transmitted from said block.

3. Sub code demodulation

(1) Sub code demodulation

Synchronizing signals S0 and S1 of 14-bit sub codes are detected out of the 23-bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output out of SCOR pin and S0 · S1 is output out of SBSO pin (only when SCOR = H).

Data (P - W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ pin, and at the same time, it is loaded in the 8-bit shift register and is output out of SBSO pin in correspondence to a clock from EXCK pin.

The details of this timing will be shown in **"1, CPU interface"**. (Page 28)

(2) Sub code Q error detection

The CRC result of sub code Q is output from the CRCF pin in synchronism with the SCOR pin.

It goes "L" when an error is detected. If the CRCQ flag is "1" at this time, the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detailed in **"1. CPU interface"**.

CIRCUIT DESCRIPTION

4. RAM interface (generation of external RAM address)

(1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal.

This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'tal system are used for processing thereafter.

(2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block.

This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock **C212 (8.4672 MHz/4)**. The data output out of the RAM is C2 pointer first, less significant 8-bit out of 16-bit and finally more significant 8-bit.

(3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data.

In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8-bit data directed to the RAM interface block from the error correction block.

The requests from the error correction unit are of the lowest priority among requests of three types.

After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal.

This block generates type address of the requested data, and controls R/W of the RAM at the same time.

(4) Address generation

The data after EFM demodulation is data subjected to interleave processing.

This interleave processing is subjected to data lag by the unit of a frame.

Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer.

The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

(5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows, beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Point R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

CIRCUIT DESCRIPTION

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum.
In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are generated simultaneously, priority is given to request 2, and if a request is generated during execution of either request, priority is given to the job in execution.

(6) Jitter margin

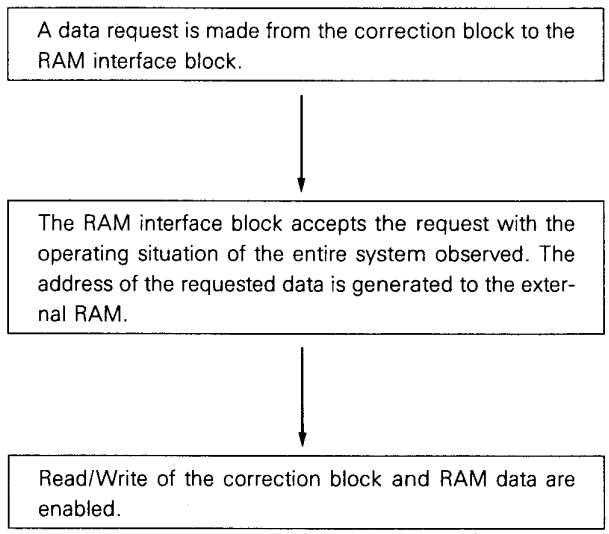
The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synchronized with the clock of X'tal system, this RAM is subjected to time axis correction.
However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.
In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter.
As a result, there is no case where data without error correction is output to the D/A.
The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

5. Error correction

(1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
(2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16K RAM stores these pointer data in addition to audio data.
(3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
(4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
(5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16-bit).
(6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
(7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" in minimum 472ns (see Note) after deactivation of pin RFCK. C2FL is the AND of C2F1 and C2F2.

Note: 472ns: One period of 2.1168 MHz

(8) The flow of data with the external RAM is as follows.



(9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output.
C1F1, C1F2, C2F1 and C2F2 output to DA01 - DA04 are these monitor signals. These signals are reset to "L" when a period of minimum 472ns has elapsed since deactivation of RFCK.
The levels and meanings of these signals at the time of deactivation of RFCK are as follows.

CIRCUIT DESCRIPTION

C1F1	C1F2	C1 correction status
0	0	No error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

6. CLV servo control

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP pin for controlling synchronization of velocity and phase, MDS pin for controlling synchronization of velocity, FSW pin for making selection of filter constant and MON pin for controlling motor ON/OFF.

(1) STOP: Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

(2) KICK: Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

(3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".

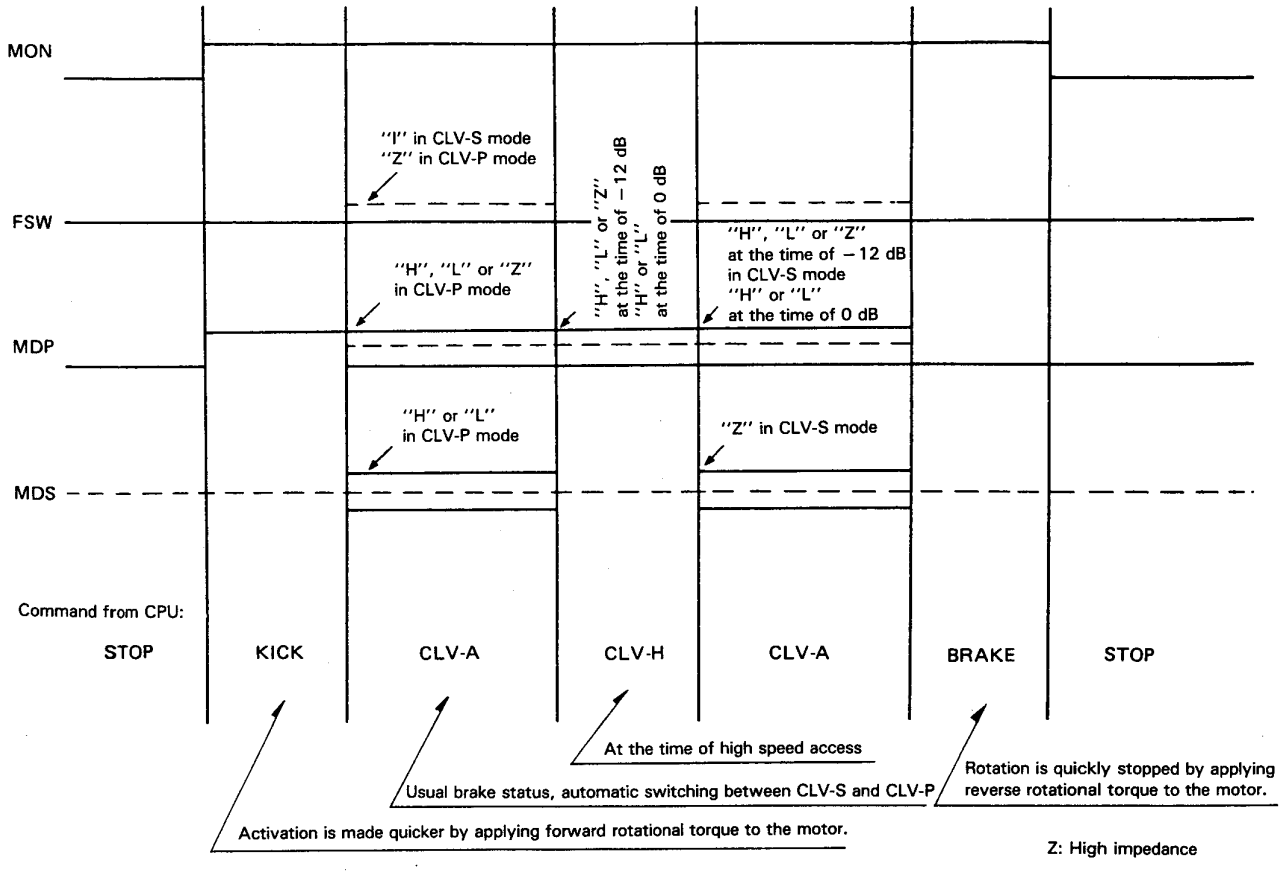


Fig. 9 Typical control of spindle motor

CIRCUIT DESCRIPTION

(4) CLV-S: Register E = 1110'B

Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason.

When the period of VCO's oscillation frequency 8.6436 MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practice, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulse are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal.

"L" is produced out of MDP pin while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more. Either 0 dB or 12 dB can be selected as its gain.

MDS = "Z", FSW = "L", MON = "H".

(5) CLV-H: Register E = 1100'B

Rough servo mode used at the time of high-speed access.

Assuming there are 20,000 tracks, from the innermost to the outermost, and that this distance is accessed in 1 second, the mirrors (portions where there are no pits) between tracks result in a 20 kHz signal, which is superimposed on the EFM signal. When such a signal is input in the CLV-S mode, a longer mirror section than the actual frame sync signal is detected as the peak value, resulting in an unstable servo.

Therefore, in order to stabilize the servo during high-speed access, the CLV-H mode performs the peak hold at a period of 8.4672/256 MHz (about 34 kHz). Then, like the CLV-S mode, it performs the bottom hold at a period of RFCK/16 or RFCK/32. Except for the period of peak detection, other operations of the CLV-H mode are the same as for the CLV-S mode.

Pwmdx: Pulse width after bottom hold
TB: Bottom hold period, i.e. RFCK/16 or RFCK/32
Z: High impedance

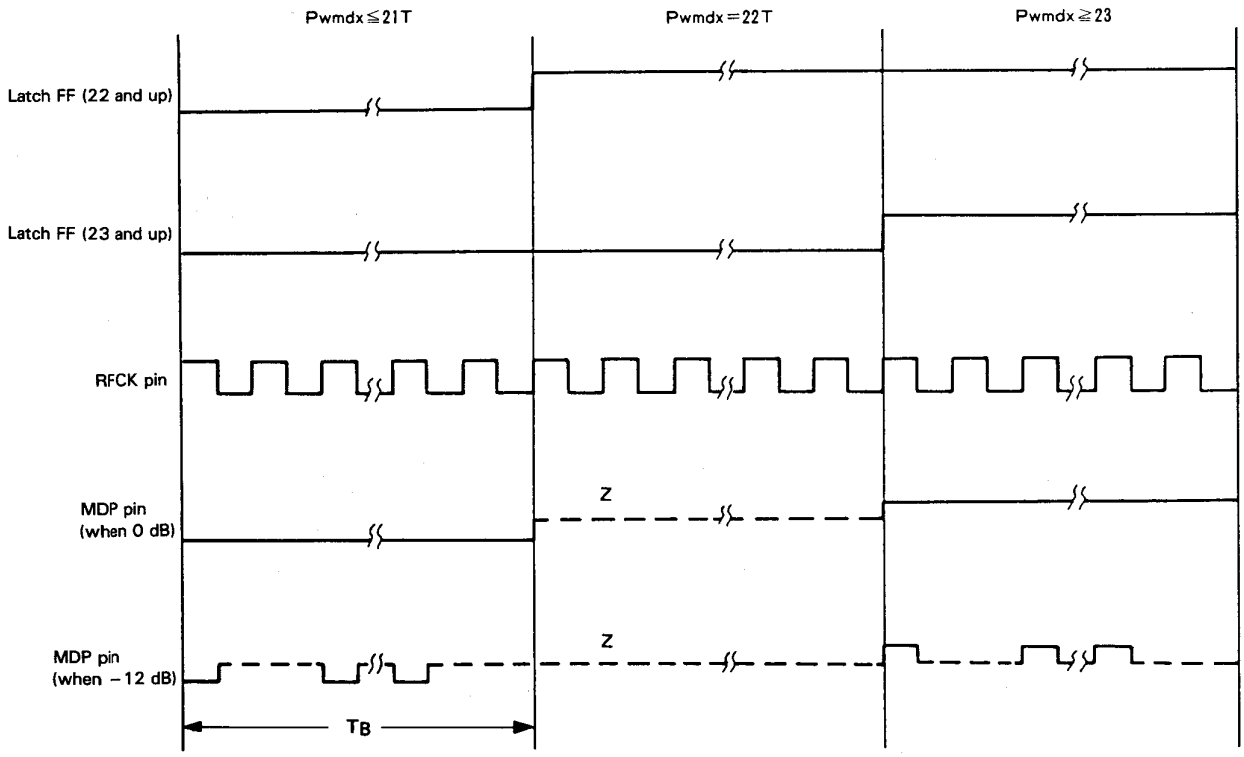


Fig. 10 Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

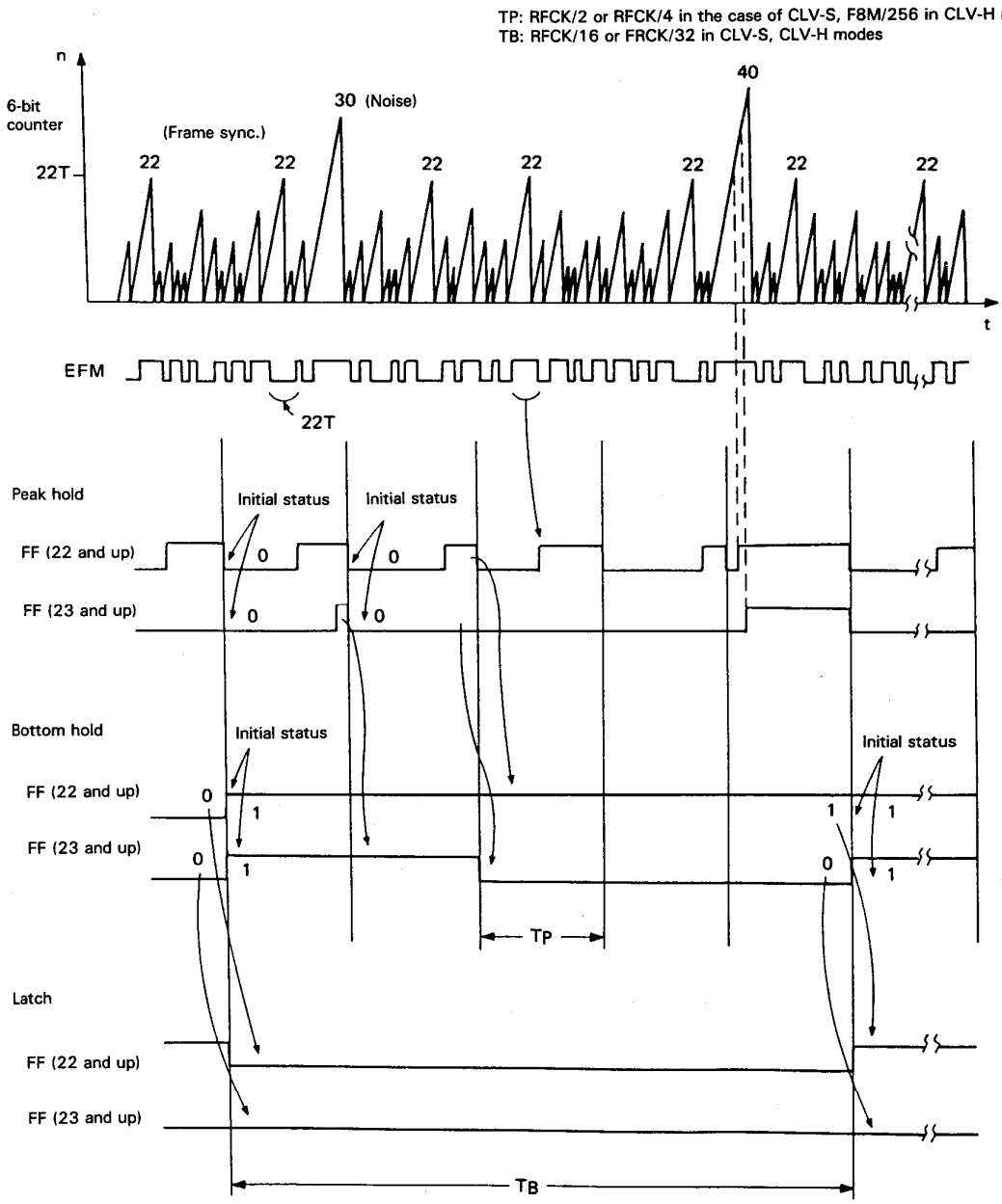
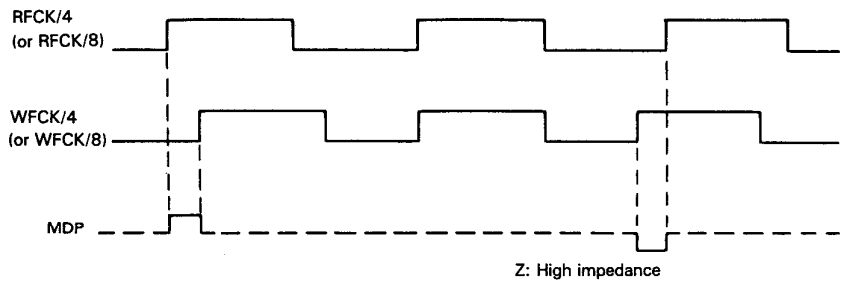


Fig. 11 Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

(6) CLV-P: Register E = 1111'B
PLL servo mode.
When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized.
Assuming the 8.4672/2 MHz period is T, and the time when WFCK is "H" is thw, the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (thw-279T) × 32, and then goes "L" until the next trailing edge of WFCK.
MDS = "H" when thw ≧ 279T,
MDS = "L" when thw ≦ 279T.
The MDS pin varies between 32T and 544T, in 32T steps, when 280T ≦ thw ≦ 296T. For example, when synchronized (rotating at the standard speed), that is when thw = 288T, a 7.35 kHz signal, with a duty cycle of 50% is output.
FSW = "Z", MON = "H".

MDP pin



5) MDS pin (The period of 4.2336 MHz is expressed as "T".)

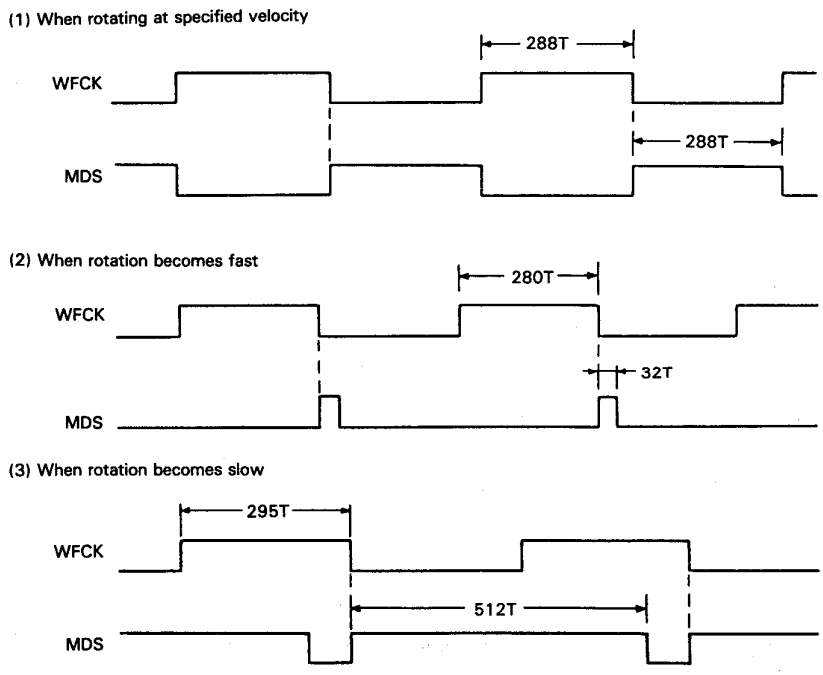


Fig. 12 Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

(7) CLV-A: Register E=0110'B

The mode used for normal play status.

The GFS signal ("H" when locked, "L" when unlocked), after frame sync detection, protection and interpolation block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is "H". When the "L" signal continues for 8 times, the mode is automatically changed to CLV-S mode.

When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is performed in register E. The description of these registers are detailed in **"1. CPU interface"**. (Page 28)

Note:

When PSSL="L", DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

(8) CLV-A': Register E=0101'B

New auto servo mode added to the CX23035.

The difference between CLV-A' and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.

The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

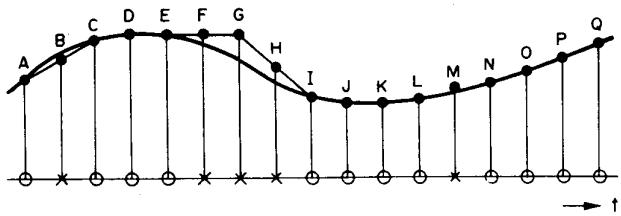
CIRCUIT DESCRIPTION

7. Interpolation and mute, attenuate

(1) Interpolation circuit block

3-byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8-bit and motor significant 8-bit. The total 16-bit constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16-bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



○: Without C2 pointer
X : With C2 pointer

Fig. 13

Mean value interpolation

$$B=\frac{1}{2}(A+C)$$

$$H=\frac{1}{2}(E+I)$$: When pointers are continuous

$$M=\frac{1}{2}(L+N)$$

Previous value hold

$$F=G=E$$

16-bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H".

C2PO signal outputs C2 pointer to the 16-bit data directed DA01 - DA16 (PSSL=H), DA16 (PSSL=L).

In other words, it means that the 16-bit data that is output when C2PO is "H", is interpolated data.

(2) Explanation of muting and attenuator

In the muting block it is possible to mute ($-\infty$ dB) or attenuate (−12 dB) the audio signal in accordance with the MUTG pin and ATTM signal of the CPU interface block.

When the ZCMT flag of register 9 is "1", the input from the MUTG pin is valid only if all of the audio data higher 6-bit (including the sign bit) are "1" or "0".

Note that switching the MUTG pin does not cause muting if the data zero-cross does not occur. To eliminate this problem, after switching the MUTG pin "H" or "L" with ZCMT="1", ZCMT shall be turned "0" in a specified period of time, regardless of whether the zero-cross causes muting ON/OFF or not.

ATTM	MUTG	Attenuation value	Remarks
0	0	0 dB	
1	0	−12 dB	
0	1	$-\infty$ dB	(See Note)
1	1	−12 dB	(See Note)

Note:
When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.
Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter value is loaded.

CIRCUIT DESCRIPTION

8. Mode setting

The various kinds of mode can be set by combining the following pins. (Refer to Table 2.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.
MD2 pin : Mainly for selection of the digital out function.
MD3 pin : Mainly for selection of the digital filter function.
PSSL pin : Mainly for selection between serial and parallel output.
SLOB pin : Selection between offset binary and 2's complement.

Input pin					Function					(Note)	Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

Note:
- **8M/16M: Selection of clock, XTAI or XTAO. 8.4672 MHz/ 16.9344 MHz**
- **DO OFF/ON: Digital out OFF/ON**
- **DF OFF/ON: Digital filter OFF/ON**
- **P/S: Parallel output/serial output**
- **OB/2's: Offset binary/2's complement**
- **CD ROM/AUDIO: Compatible to CD ROM/Compatible to audio**

Table 2

• Selection of clock

The oscillator clock for XTAI and XTAO is available at 16.9344 MHz and 8.4672 MHz. However, when digital output is used, the clock must be set to 16.9344 MHz.

• Selection of digital filter (Refer to "9. Digital filter".)

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

• Selection of parallel output/serial output

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data.

When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

C1F1 (DA01) :
C1F2 (DA02) : Error correction status monitor output at C1 decode.
C2F1 (DA03) :
C2F2 (DA04) : Error correction status monitor output at C2 decode.
C2FL (DA05) : Correction status output, C2FL = C2F1·C2F2.
C2PO (DA06) : C2 pointer signal.
RFCK (DA07) : Read frame clock signal, 7.35 kHz when locked to the crystal line.
WFCK (DA08) : Write frame clock signal, 7.35 kHz when locked.
$\overline{\text{PLCK}}$ (DA09) : 1/2 of the divided signal from the VCO pin, 4.3218 MHz when locked.
UGFS (DA10) : Non-protected frame sync signal.
GTOP (DA11) : Frame sync protect status display signal.
RAOV (DA12) : Jitter margin over or underflow display signal.
C4LR (DA13) : 4 times the LRCK signal.
$\overline{\text{C210}}$ (DA14) : Bit clock (invert signal of $\overline{\text{C210}}$).
C210 (DA15) : Internal system clock (4.2336 MHz when DF is ON, 2.1168 MHz when CXD1125Q or DF is OFF).
DATA (DA16) : Serial data output (MSB or LSB first output).

CIRCUIT DESCRIPTION

• Selection of offset binary/2's complement

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

• Selection of CD ROM/audio compatibility

When MD1 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8-bit of the 16-bit, only the C2 pointer corresponding to the upper 8-bit goes "H", and the lower 8-bit are processed as the correct data.

9. Digital filter

The built-in digital filter has the following features:

1. Correction of the aperture effect
2. Small attenuation at 20 kHz
3. Practical-design filtering band ranges

(1) Filter characteristics

Passing Band	Ripple from DC to 18 kHz	±0.07 dB max.
	Attenuation of 20 kHz with respect to 1 kHz	0.65 dB max.
Filtering Band	Attenuation of 44.1 ± 1 kHz with respect to 1 kHz	87 dB min.
	Attenuation of 44.1 ± 5 kHz with respect to 1 kHz	58 dB min.
	Attenuation of 44.1 ± 10 kHz with respect to 1 kHz	44 dB min.
	Attenuation of 44.1 ± 20 kHz with respect to 1 kHz	10 dB min.
	Frequency range in which attenuation is −30 dB with respect to 1 kHz	44.1 ± 14 kHz
	Frequency range in which attenuation is −60 dB with respect to 1 kHz	44.1 ± 4 kHz

10. Countermeasures to defect

To counter a defect, the PDO pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after about 0.55 ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".
The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK Pin.

After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".
This operation is similar to that for the FSW pin.
However, while the FSW outputs a fixed signal when not in CLV-A or CLV-A' mode, the LOCK pin always output the above signal.

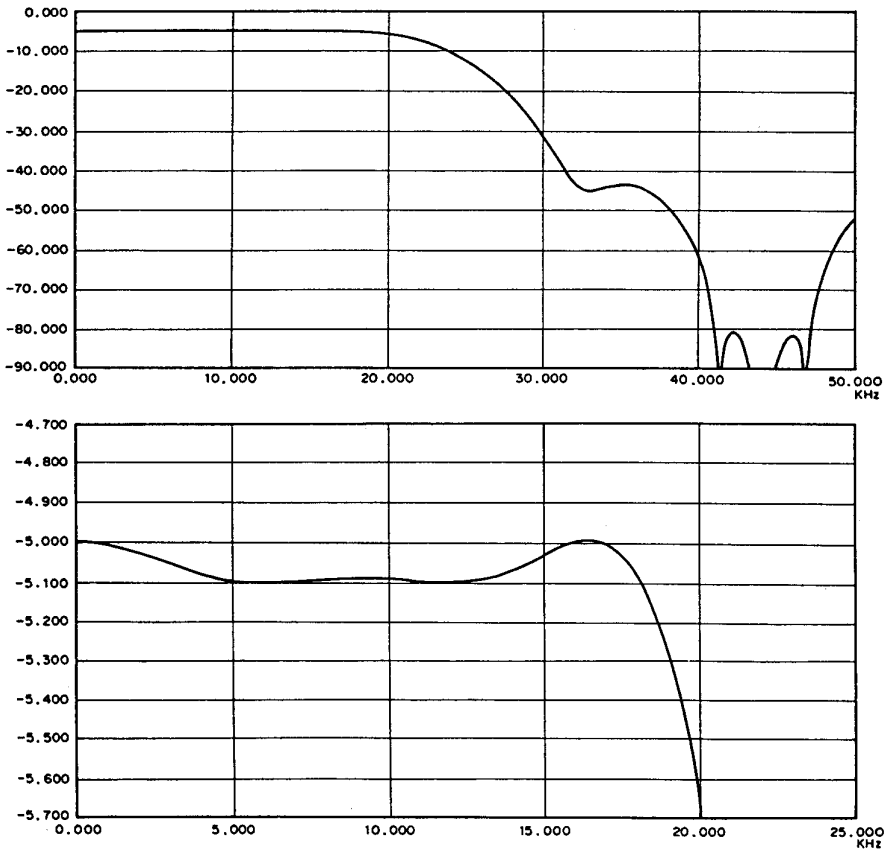
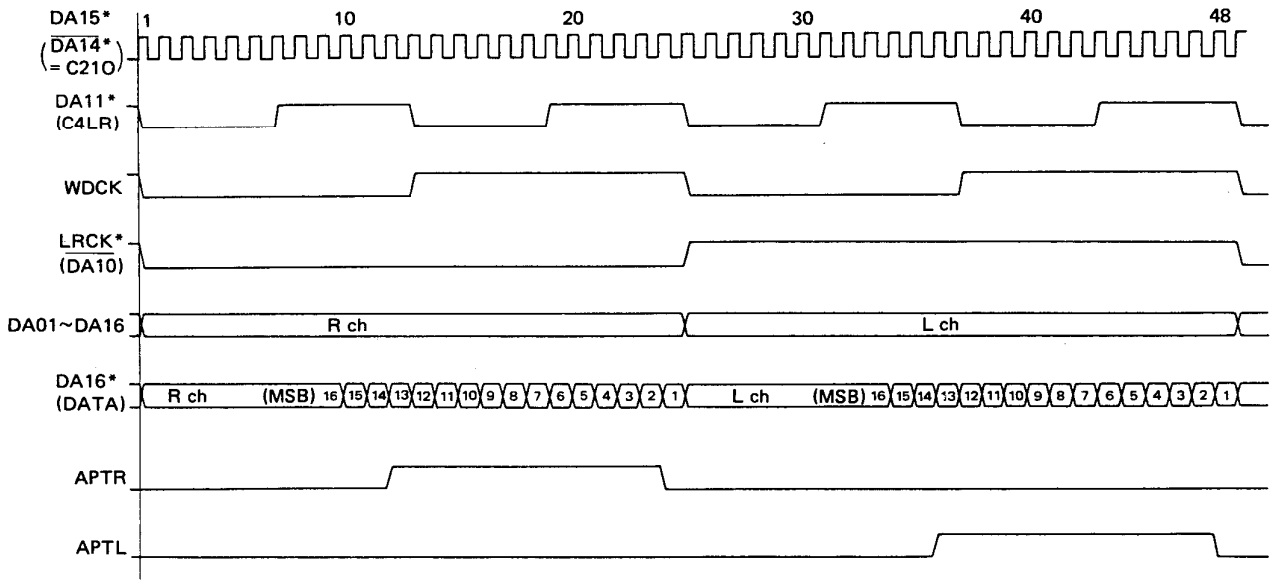


Fig. 14 Frequency characteristic after sample & hold

CIRCUIT DESCRIPTION

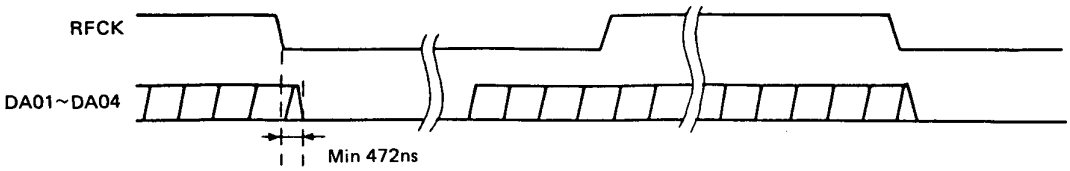
• **Timing chart**



* When PSSL = "L".

Fig. 15 Timing chart of audio output

CIRCUIT DESCRIPTION



* DA01 to DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* AND signal of C2F1 and C2F2 is output out of C2FL pin.

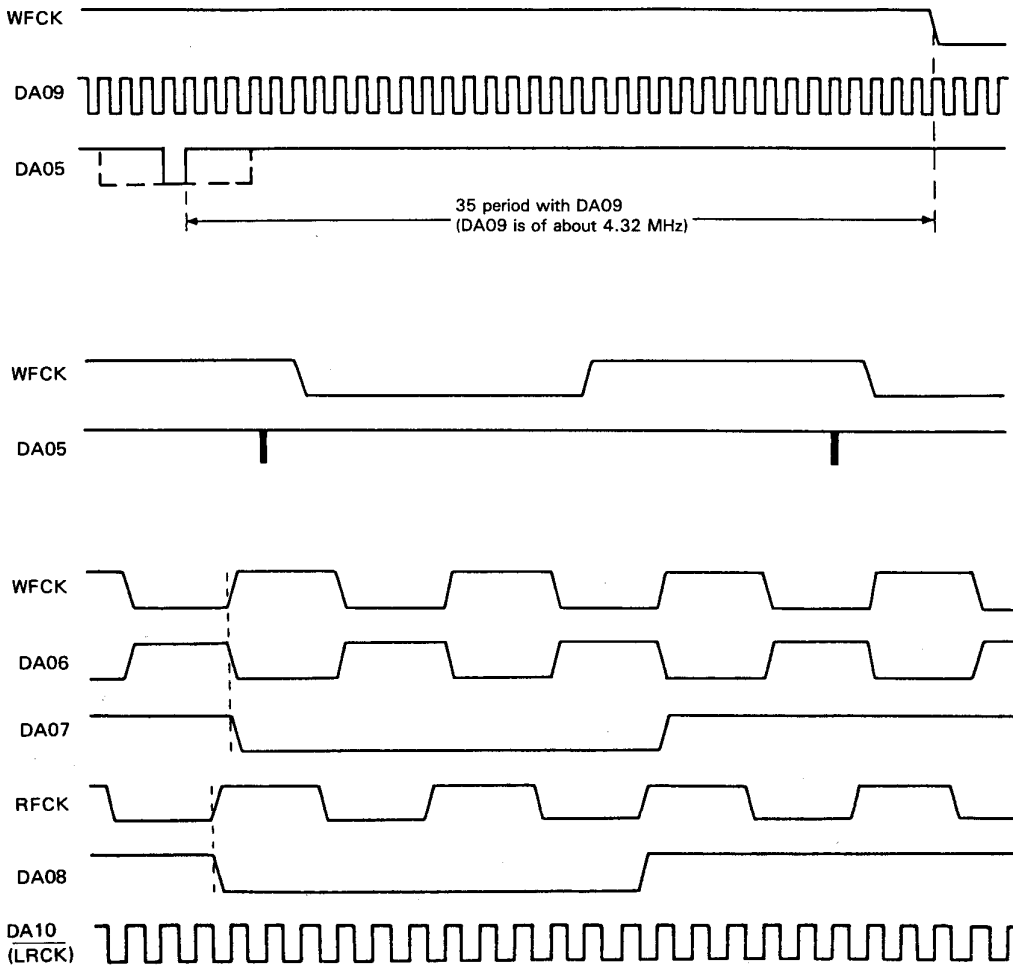


Fig. 16 Timing chart of DA01 to DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION

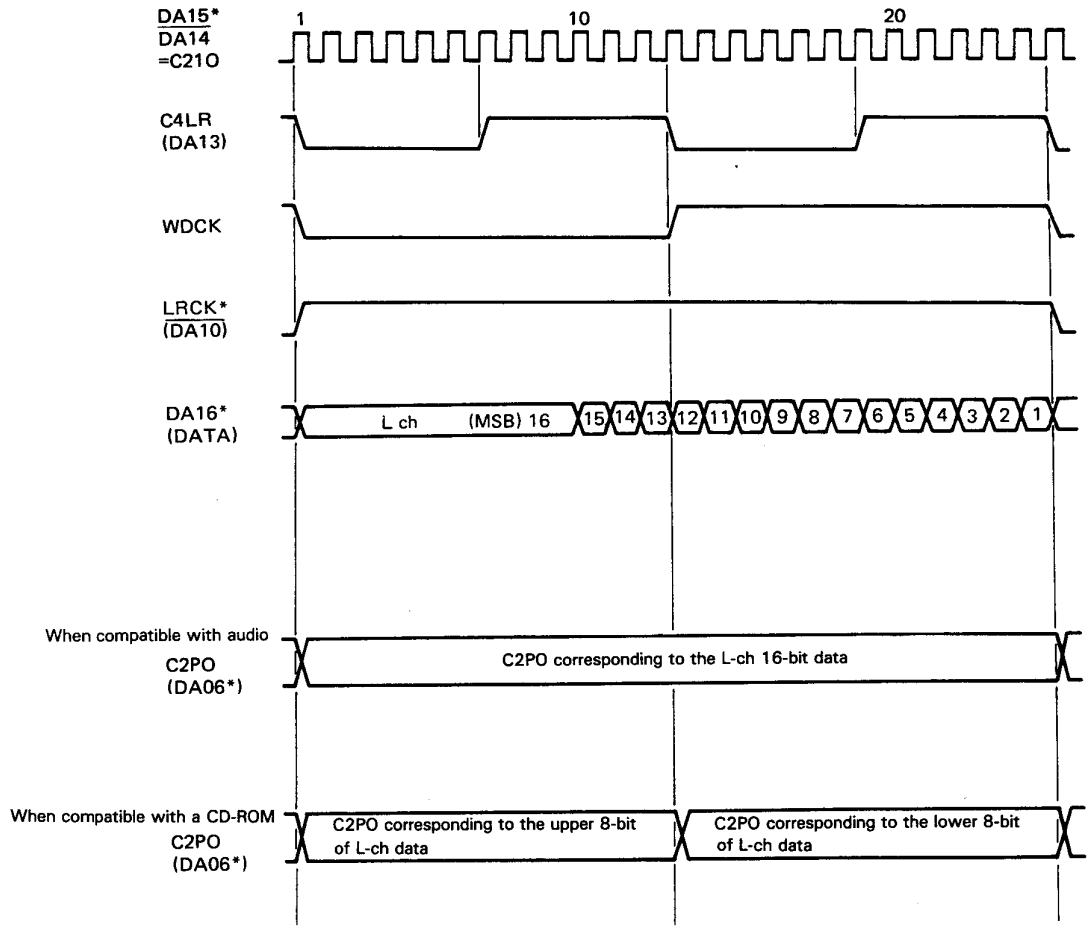


Fig. 17 Timing chart of C2PO output (when PSSL = "L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

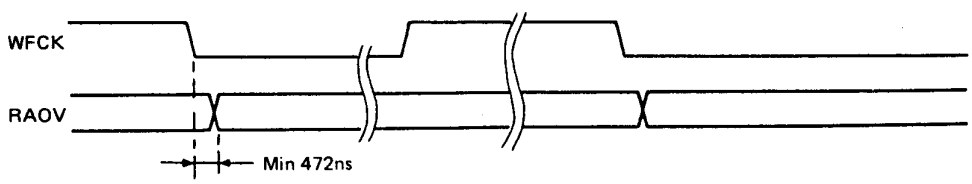


Fig. 18 Timing chart of RA0V output

CIRCUIT DESCRIPTION

U403: CMOS 4-BIT, 1-CHIP MICROPROCESSOR (CXP5024Q)

General

The CXP5024Q is a CMOS 4-bit microprocessor, which incorporates a 4-bit CPU, ROM, RAM, I/O ports, an 8-bit timer, an 8-bit timer/counter, an 18-bit time base timer, an 8-bit serial I/O, a vector interrupt function and a power-on reset function, as well as an LCD controller/driver and a standby function for low power consumption, in a single chip.

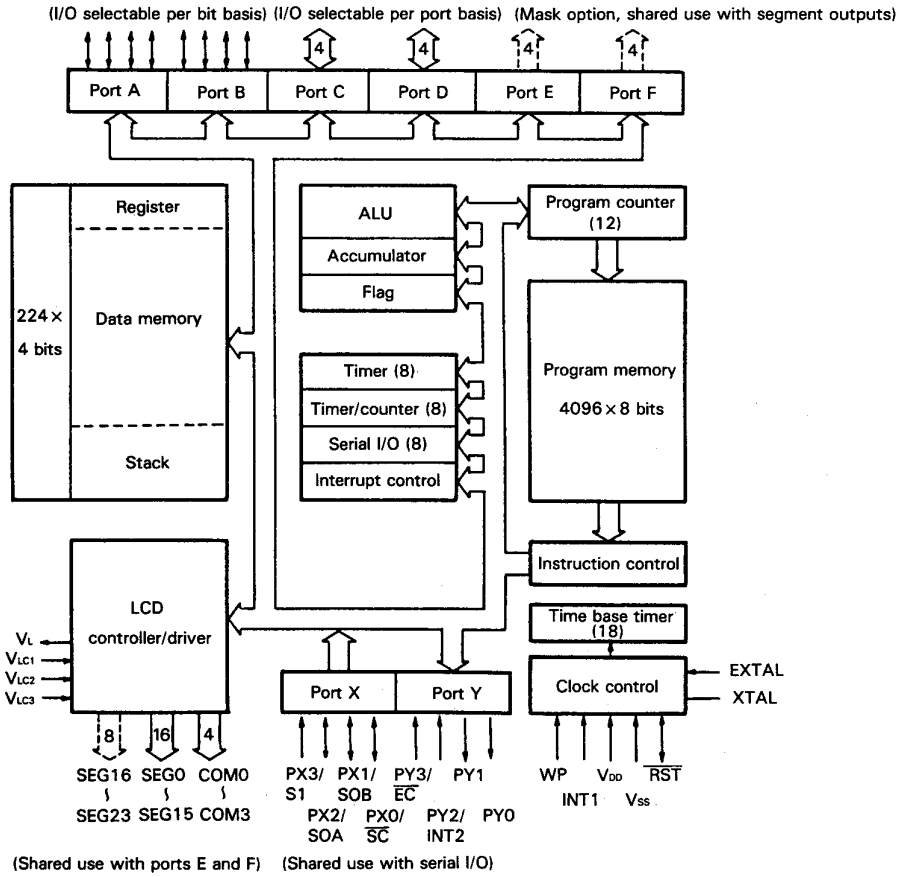
Features

- Basic instruction cycle: 3.8 μs/4.19 MHz, 1.9 μs/4.19 MHz (High-speed version)
- ROM capacity: 4,096×8 bits
- RAM capacity: 224×4 bits (24×4 bits of which are also used as an LCD display memory)
- General-purpose I/O ports with 32 lines (16 of which are used for segment output)
- LCD controller/driver with direct-drive capability.
  The segment output lines can optionally be selected to 24, 20 or 16.
  The duty cycle is programmable to 1/3 or 1/4.
  1/3 bias.
- Two external interrupt terminals.
- 8/4-bit variable serial I/O.
- Independently-controllable 8-bit timer, 8-bit timer/event counter and 16-bit time base timer.
- Arithmetic and logic operations between all RAM and I/O areas, and an accumulator using memory-mapped I/O.
- Reference to all ROM area using table look-up instructions.
- Two power-down modes: Sleep, Stop.
- Power-on reset circuit.
- Either crystal or CR oscillator can be selected optionally.

Structure

Silicon gate CMOS IC

Block diagram



CIRCUIT DESCRIPTION

Terminal explanations

Terminal No.	Terminal name	I/O	Signal name	Active H/L	Function
1	PY0	O	POWER ON/OFF	H OFF L ON	POWER ON/OFF signal.
2	PY1	O	MUTG	H ON L OFF	Muting output. In normal operation, MUTG is "L" when internal register ATTM is "L".
3	INT2/PY2	I	LIMIT SW	H OUT L IN	Innermost limit switch input.
4	$\overline{EC}$/PY3	O	SENCE		Internal status output according to address.
5	$\overline{SC}$/PX0	O	SQCK	⌐↑	Sub code Q read clock.
6					
7					
8	SI/PX3	I	SUBQ		Sub code Q input.
9	PD0	O	EMPHA	H ON L OFF	Disc emphasis ON/OFF signal.
10	PD1	O	LASER	L ON H OFF	Laser ON/OFF signal.
11	PD2	O	HIFILTER	H ON L OFF	Hi-Filter ON/OFF signal.
12	PD3	O	SOUND	H OFF L ON	Sound ON/OFF signal.
13	PC0	I	KIN3		MSB Key latch input port. LSB
14	PC1	I	KIN2		
15	PC2	I	KIN1		
16	PC3	I	KIN0		
17	PB0	I	FOK	H OK L NG	Focus OK signal.
18	PB1	I	GFS	H LOCK L UNLOCK	Frame sync lock status display input.
19	PB2	I	OPEN/CLOSE	H OPEN L CLOSE	Open/Close signal.
20	PB3	I	LOW BATT	H L LOW	Battery voltage alarm signal.
21	PA0	I	TEST TP	H NORMAL L TEST	Microprocessor test mode activation terminal. (0 V)
22	PA1	O	KS1	L LATCH	Key latch output port.
23	PA2	O	KS2		
24	PA3	O	KS3		
25	V_{SS}		V_{SS}		GND (0V).
26	V_{DD}		V_{DD}		Power supply. (+5 V)
27	PE3 SEG23	O	$\overline{XRST}$	L	System reset output.
28	PE2 SEG22	O	DATA		Serial data output from the CPU.
29	PE1 SEG21	O	XLT	⌐⌐	Latch output from the CPU.

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Signal name	Active H/L	Function
30	PE0 SEG20	O	CLK		Clock output for serial data transfer from the CPU.
31	SEG19 PF3	O	SEG19		Display segment outputs.
32	SEG18 PF2	O	SEG18		
33	SEG17 PF1	O	SEG17		
34	SEG16 PF0	O	SEG16		
35	SEG15	O	SEG15		
36	SEG14	O	SEG14		
37	SEG13	O	SEG13		
38	SEG12	O	SEG12		
39	SEG11	O	SEG11		
40	SEG10	O	SEG10		
41	SEG9	O	SEG9		
42	SEG8	O	SEG8		
43	SEG7	O	SEG7		
44	SEG6	O	SEG6		
45	SEG5	O	SEG5		
46	SEG4	O	SEG4		
47	SEG3	O	SEG3		
48	SEG2	O	SEG2		
49	SEG1	O	SEG1		
50	SEG0	O	SEG0		
51	COM3	O	COM3		Common display segment outputs.
52	COM2	O	COM2		
53	COM1	O	COM1		
54	COM0	O	COM0		
55					
56					
57					
58	V_{DD}		V_{DD}		Power supply. (+5 V)

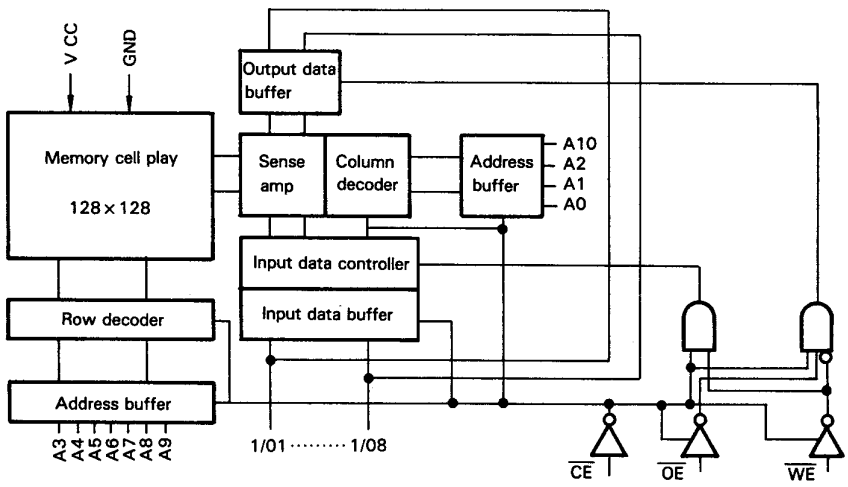
CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Signal name	Active H/L	Function
59					
60	XTAL	O	XTAL		X'tal oscillator output. (f=8.4672 MHz or 16.9344 MHz)
61	EXTAL	I	EXTAL		
62	$\overline{RST}$	I	RESET	L	Microprocessor reset input.
63					
64	INT1	O	SCOR	⎍↑	Sub code sync S0+S1 output.

U402: STATIC RAM (LC3517ALM-15)

Function
2048-word x 8-bit static RAM
Application
Memory system, battery-driven portable system

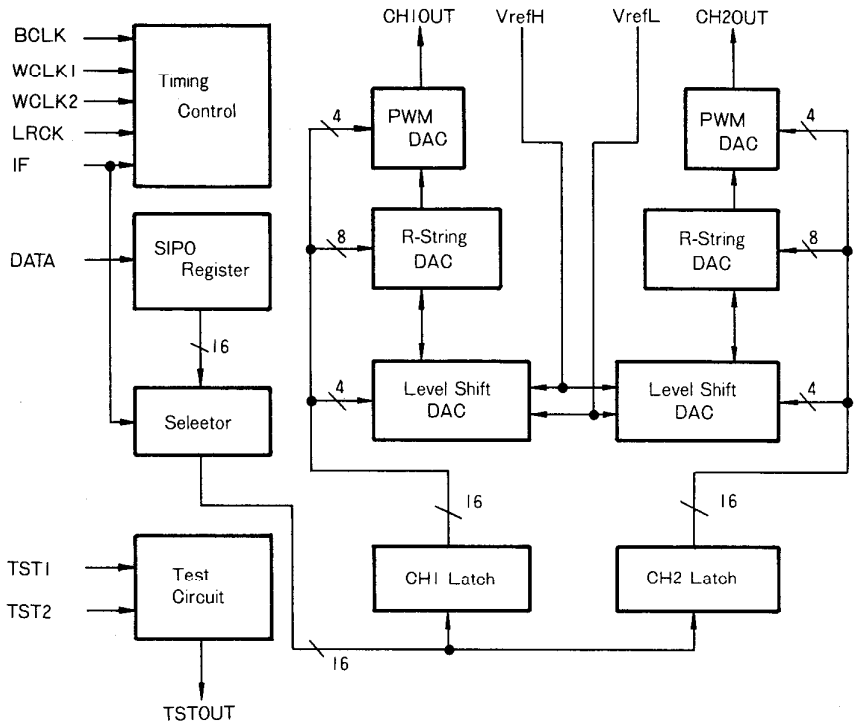
Block diagram



CIRCUIT DESCRIPTION

U501: 16-BIT D/A CONVERTER (LC7880M)

Block diagram



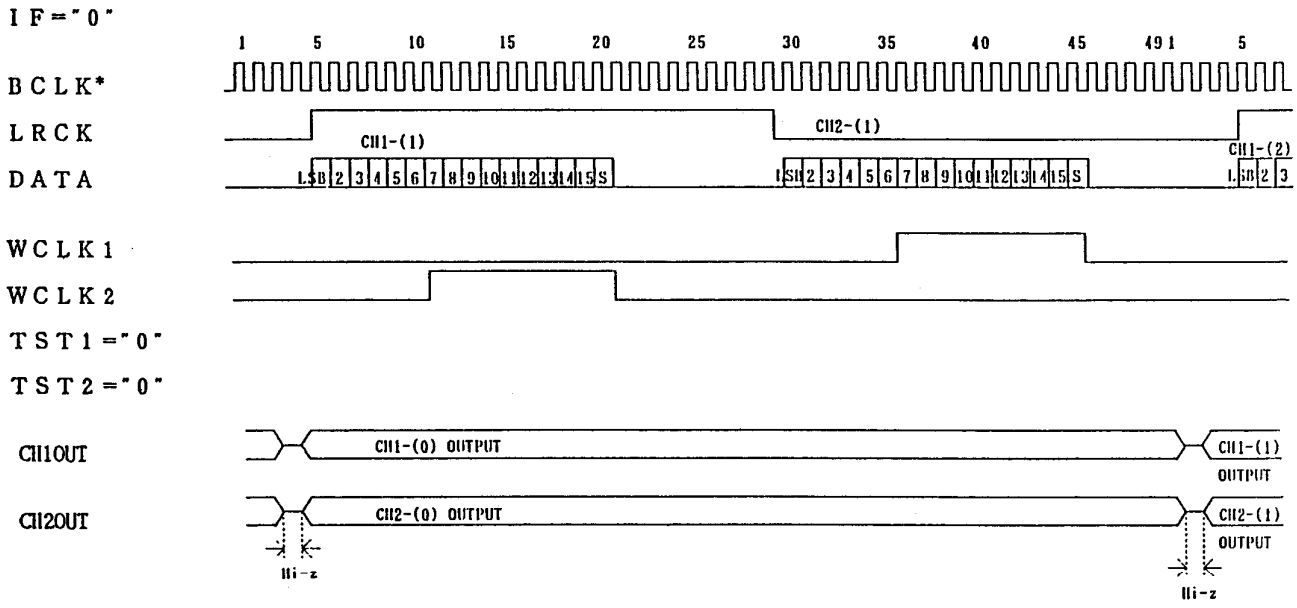
CIRCUIT DESCRIPTION

Terminal explanations

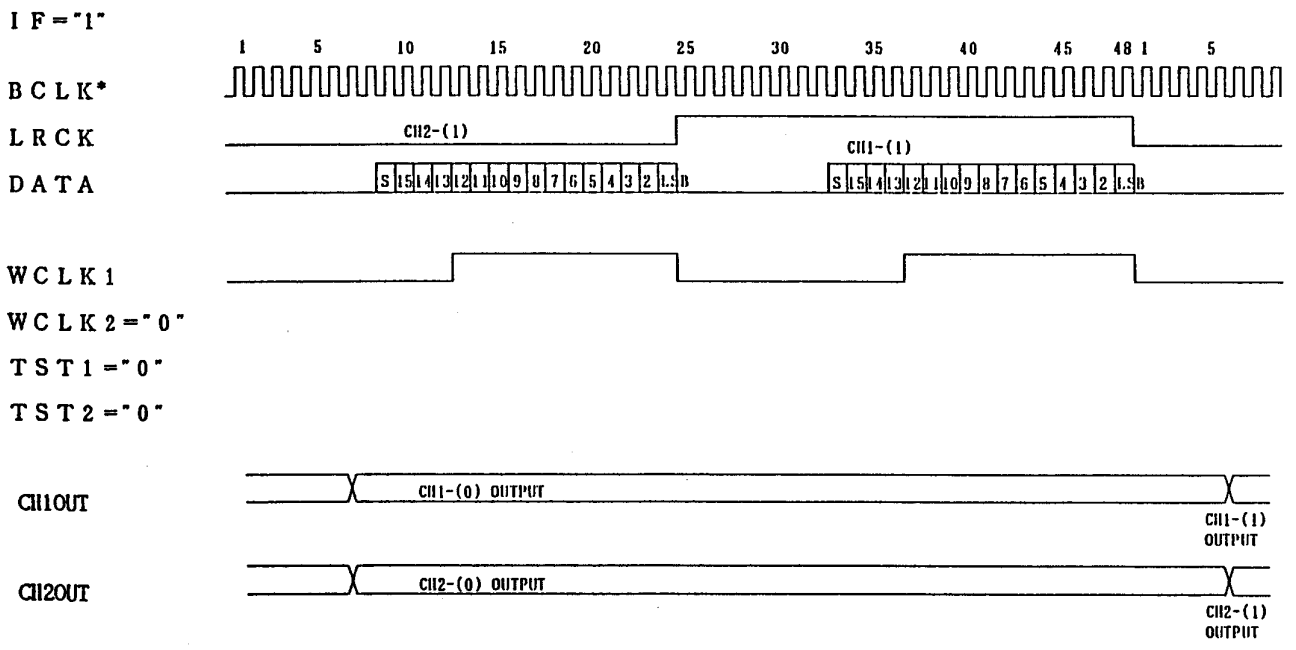
Terminal No.	Terminal name	Function
1	CH1 OUT	CH1 output pin. (R-ch when combined with LC7860).
2	Vref H	Reference voltage "H" input pin.
3	NC	No connection.
4	V_{DD}	Supply voltage pin. (+5 V)
5	WCLK2	Word clock 2 input pin. When IF is an "L" level, the trailing edge of WCLK2 is used to generate an internal signal for latching the digital audio CH1 data. When IF is an "H" level, WCLK2 will also be set to an "L" level.
6	LRCK	LR clock input pin. Indicates whether the input digital audio data is from CH1 or CH2. It is CH1 when LRCK is an "H" level, and CH2 when LRCK is an "L" level.
7	WCLK1	Word clock input pin. When IF is an "L" level, the trailing edge of WCLK1 is used to generate an internal signal for latching the digital audio CH2 data. When IF is an "H" level, the trailing edge of WCLK1 is used to generate an internal signal for latching both the digital audio CH1 and CH2 data.
8	DATA	Digital audio data input pin. When IF is an "L" level, data is input in bit serial form from the LSB. When IF is an "H" level, data is input in bit serial form from the MSB.
9	BCLK	Bit clock input pin. The bit clock is used to read bit-serial digital audio data in the LSI, and is also used as the PWM DAC clock.
10	V_{DD}	Supply voltage pin. (+5 V)
11	TSTOUT	Test output pin. Connected to GND in normal modes.
12 13	TST1 TST2	Test input pin. Connected to GND in normal modes.
14	IF	Interface switching pin. When IF is an "L" level, the digital audio data input format is LSB first. When IF is an "H" level, the digital audio data input format is MSB first.
15	GND	GND pin.
16	Vref L	Reference voltage "L" input pin.
17	GND	GND pin.
18 19	NC	No connection.
20	CH2 OUT	CH2 output pin. (L-ch when combined with LC7860).

CIRCUIT DESCRIPTION

Timing charts



* BCLK=4.3218MHz (Fs=88.2kHz)
=2.1609MHz (Fs=44.1kHz)



* BCLK=4.2336MHz (Fs=88.2kHz)
=2.1168MHz (Fs=44.1kHz)

ADJUSTMENT

No.	ITEM	INPUT SETTINGS	OUTPUT SETTINGS	PLAYER SETTING	ALIGNMENT POINTS	ALIGN FOR	FIG.
Remove the cover(bottom panel).							
1	PLL	–	Connect ASY terminal to GND and connect a frequency counter to PLL terminal.	PLAY	RV301 (X25-3090-00)	4.26MHz	(a)
2	FOCUS OFFSET (1)	Test disc (Type 4)	Connect an oscilloscope to FE terminal.	PLAY	–	Check DC voltage.	(b)
3	FOCUS OFFSET (2)	Test disc (Type 4)	Connect an oscilloscope to FE terminal.	STOP	RV102 (X25-3100-00)	Shall be the same as above.	(b)
Repeat (2) and (3) to ensure there is no difference in voltages.							
4	TRACKING BALANCE	Test disc (Type 4)	Connect an oscilloscope to TE terminal.	Play disc and enter test mode. (by connecting TEST terminal to GND, supply +5V to the right TEST terminal, then unsolder bridge at D307)	RV101 (X25-3100-00)	Waveform shall be symmetrical above and below 0 V. DC = 0 ±10 mV	(c)
5	TRACKING GAIN	Test disc (Type 4)	Connect an AC voltmeter to TRACK terminal and an AG (1 kHz, 0.2V) to TE terminal.	PLAY	RV302 (X25-3090-00)	Assuming the point where servo is applied is 0 dB, set the disturbance signal (1 kHz) to -5 dB ±1 dB.	(d)

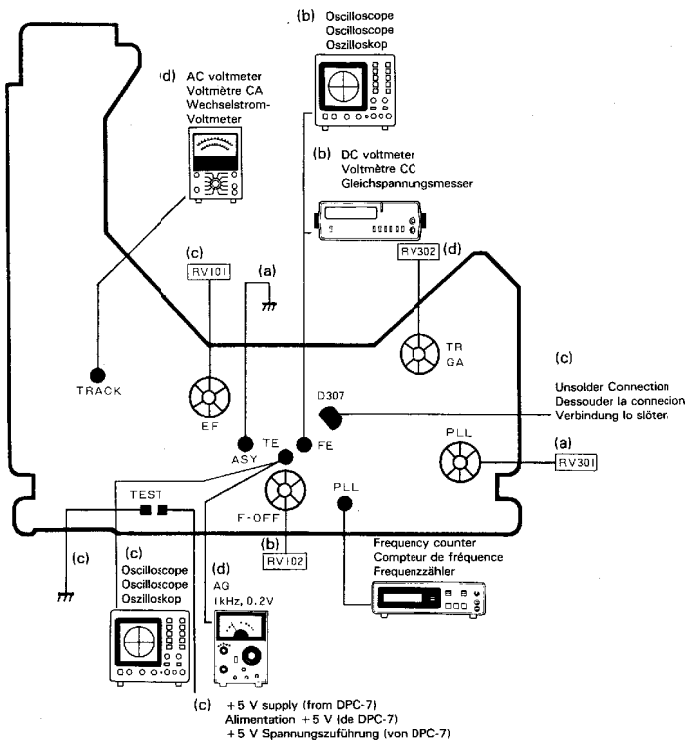
REGLAGES

N°	ITEM	REGLAGE DE L'ENTREE	REGLAGE DE LA SORTIE	REGLAGE DE LA LECTURE	POINTS L'ALIGNMENT	ALIGNER POUR	FIG.
Retirer le couvercle(panneau du dessous).							
1	PLL	–	Raccorder la borne ASY à GND et raccorder un compteur de fréquence à la borne PLL.	PLAY	RV301 (X25-3090-00)	4.26MHz	(a)
2	OFFSET DE MISE AU POINT (1)	Disque test (Type 4)	Raccorder un oscilloscope à la borne FE.	PLAY	–	Vérifier la tension CC.	(b)
3	OFFSET DE MISE AU POINT (2)	Disque test (Type 4)	Raccorder un oscilloscope à la borne FE.	STOP	RV102 (X25-3100-00)	Doit être identique à ci-dessus.	(b)
Répéter (2) et (3) pour s'assurer qu'il n'y a pas de différence dans les tensions.							
4	BALANCE D'ALIGNEMENT	Disque test (Type 4)	Raccorder un oscilloscope à la borne FE.	Lire le disque et entrer en mode de test.(en raccordant la borne TEST à GND, fournir +5V à la borne TEST de droite puis dessouder le pont à D307)	RV101 (X25-3100-00)	La forme d'onde doit être symétrique au dessus et en dessous de 0 V. CC = 0 ±10 mV.	(c)
5	GAIN D'ALIGNEMENT	Disque test (Type 4)	Raccorder un voltmètre CA à la borne TRACK et un AG (1kHz, 0.2V) à la borne TE.	PLAY	RV302 (X25-3090-00)	le point ou l'asservissement est appliqué est de 0 db, régler le signal de perturbation (1kHz) sur -5 dB ±1 dB.	(d)

ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUNG	AUSGANGS-EINSTELLUNG	SPIELER-EINSTELLUNG	ABGLEICH-PUNKTE	ABGLEICHEN FÜR	ABB.
Die Abdeckung(Bodenplatte) entfernen.							
1	PLL	–	Die ASY-Klemme mit GND verbinden und einen Frequenzzähler an die PLL-Klemme anschließen.	PLAY	RV301 (X25-3090-00)	4.26MHz	(a)
2	FOKUS-VERSATZ (1)	Testdisc (Typ 4)	Ein Oszilloskop an die FE-Klemme anschließen.	PLAY	–	Die Gleichspannung prüfen.	(b)
3	FOKUS-VERSATZ (2)	Testdisc (Typ 4)	Ein Oszilloskop an die FE-Klemme anschließen.	STOP	RV102 (X25-3100-00)	Muß gleich wie oben sein.	(b)
(2) und (3) wiederholen, um sicherzustellen, daß kein Unterschied in der Spannung besteht.							
4	SPURHALTE-BALANCE	Testdisc (Typ 4)	Ein Oszilloskop an die TE-Klemme anschließen.	Eine Disc wiedergeben und den Testmodus aktivieren. (druch Verbinden der TEST-Klemme mit GND +5V an die rechte TEST-Klemme anlegen und dann die Brücke bei D307 loslöten)	RV101 (X25-3100-00)	Die Wellenform muß über und unter 0 V symmetrisch sein. Gleichstrom = 0±10 mV	(c)
5	SPURHALTE-VERSTÄRKUNG	Testdisc (Typ 4)	Ein Wechselstrom-Voltmeter an die TRACK-Klemme und ein AG (1kHz, 0.2 V) an die TE-Klemme anschließen.	PLAY	RV302 (X25-3090-00)	Unter Annahme des Punktes, wo Servo angewendet wird, als 0 dB das Störsignal (1kHz) auf -5 dB ±1 dB einstellen.	(d)

ADJUSTMENT/REGLAGES/ABGLEICH



TROUBLESHOOTING

EXPLANATION OF OPERATIONS

1. **Supply power to the set from an AC adapter or rechargeable battery.**
2. **Switch the POWER ON.**
3. a) When the lid is open, the display is: 0 (1 digit of the track No.)
   b) When the lid is closed, the display is: 00'00"00 (flashing)
4. **Operation of the mechanism**
   a) Operation of the sled
   When the innermost limit switch is ON, the sled moves toward the outer tracks by about 1 cm, turning the limit switch ON, then moves toward the inner tracks, again turning the limit switch ON, then stops.
   When the innermost limit switch is OFF, the sled moves toward the inner tracks until the limit switch is turned ON.
   b) After operation a), the spindle motor starts rotating (about 5 sec).
5. **Operation of the laser pickup**
   a) At the same time as the disc motor starts rotating, the laser light is emitted. If no disc has been loaded, the focus search operation is repeated 3 times.
   b) If there is a disc loaded, the first focus search turns the focusing ON, the focusing servo as well as the tracking servo is applied, the lead-in data is read, the number of tracks and total playing time of the disc are displayed, and the player enters standby mode.
6. **Play skip and FF (REV) operations**
   Based on a calculation of the time difference between the present position and the destination position, the destination position is located from the combination of the sled operation and tracking track jump operation. A FF (or REV) operation is performed based on the combination of the track jump operation and the sled operation, which is caused by the generation of a tracking DC voltage.

TROUBLESHOOTING EXPLANATION

※1 Laser diode check method
First check that the laser is emitting. (Do not view the laser light directly.)
Without loading a disc, put the player in play mode and ensure that the pickup lens moves up and down for 4 seconds. Check that the laser light is emitted during this up and down movement.

※2 Focus search
With the lid open, switch the OPEN/CLOSE switch forcibly to ON. At this time, the pickup should move from the outer tracks to the inner tracks, and the lens should move up and down. If these do not occur, check the OPEN/CLOSE switch and the limit switch.

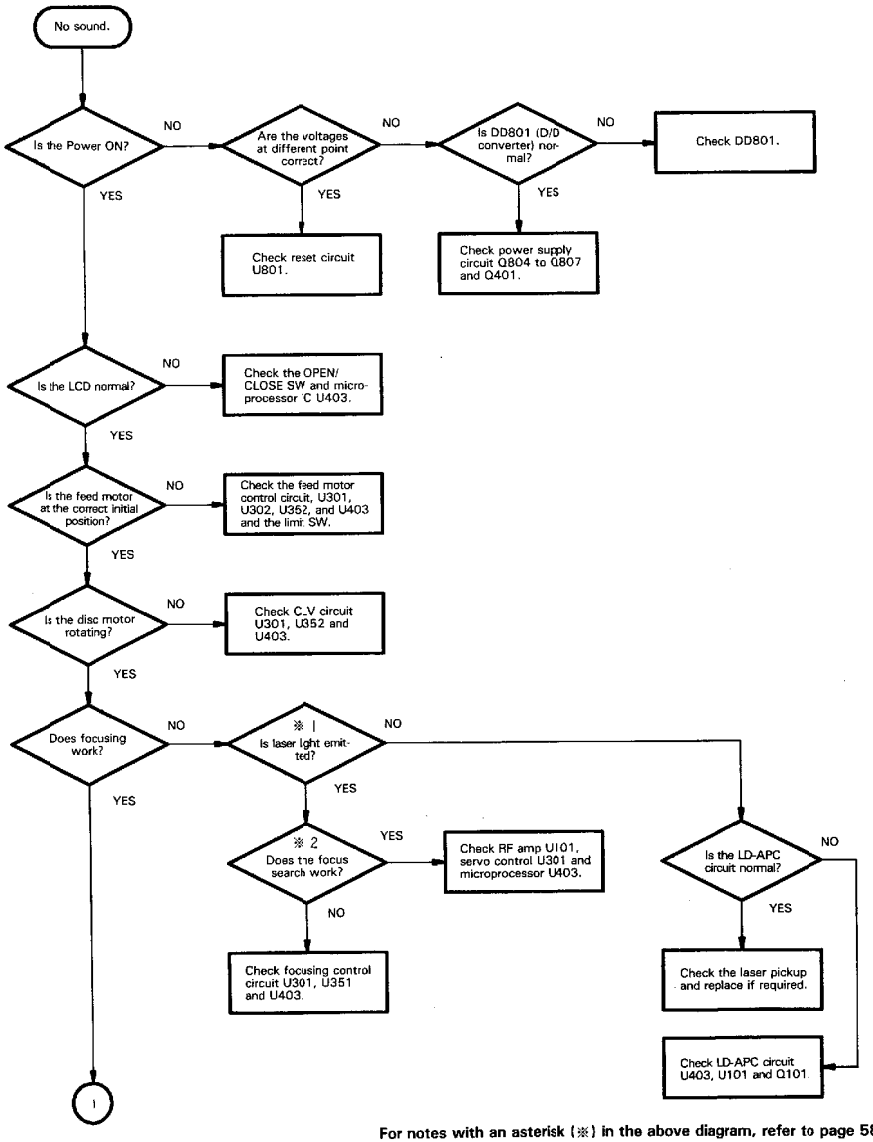
※3 GFS signal
When the frame sync judging point (U403 pin 18) is locked, the GFS (Guard Frame Synchronous) pin goes to an "H" level.

※4 Limit switch position
Load a Type 4 test disc, and check the position after the TOC has been read.
Connect the TEST pin to GND, display the track time, and set the time display to between 4:00 and 5:20.

※5 Defective disc
If a defective disc cannot be played when the player is operating is normally, check the following:
1. Visually check the disc for dirt, pinholes, etc., then play a proper disc and check the RF signal.
2. Check the tracking servo signal waveform to see if the disc is not eccentric.
3. Other
   The warp of a disc or the focusing error of a disc can be checked with the focus tracking signal.
   When the disc is normal, the horizontal and vertical movement should be less than 0.3 mm. If it exceeds this, check the disc table.

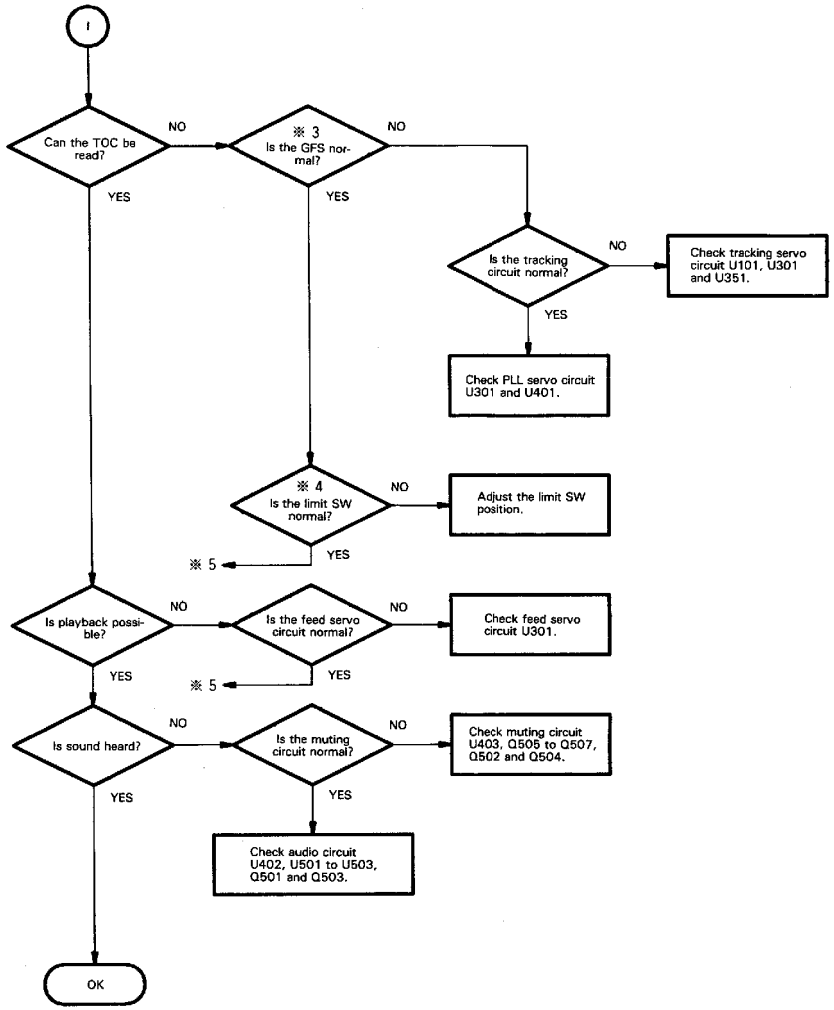
Note: Numbers marked with an ※ correspond to numbers marked with an ※ in "Troubleshooting".

TROUBLESHOOTING



For notes with an asterisk (※) in the above diagram, refer to page 58.

TROUBLESHOOTING



For notes with an asterisk (※) in the above diagram, refer to page 58.

DPC-7 DPC-7

VOLTAGE TABLE

X25-3100-00

U501

1	(2.5V)	9	
2	3.3V	10	4.3V
3	0V	11	0V
4	4.3V	12	
5	0V	13	
6		14	4.3V
7		15	0.7V
8	(0V)	16	1.8V
		17	0V
		18	
		19	
		20	(2.5V)

U351

1	0V	14	
2	2.2V	15	0V
3	0V	16	
4		17	4.5V
5		18	
6	1.0V	19	0V
7		20	
8	3.6V	21	4.6V
9	0V	22	0V
10	2.4V		
11	2.2V		
12	0V		
13	4.5V		

U101

1		13	1.7V (2.2V)	25	0V
2		14	2.2V	26	2.2V
3	2.2V	15	1.0V	27	(0V)
4	3.2V	16	1.5V (3.2V)		
5	3.3V (0V)	17	0V	28	4.5V (0V)
6	0V	18	2.2V	29	1.2V (4.5V)
7		19		30	4.4V
8	2.2V	20			
9		21	0V		
10		22			
11	2.2V	23	2.4V (1.8V)		
12	1.4V (2.2V)	24	2.0V		

U352

1	0V	14	
2	2.4V	15	0V
3	0V	16	
4		17	4.5V
5		18	
6	1.0V	19	0V
7		20	
8	3.5V	21	0V
9	0V	22	
10	2.5V (2.3V)		
11	2.2V		
12	0V		
13	4.5V		

Q504L

E	0V
C	–
B	–

Q804

E	4.6V
C	–
B	–

Q501R

E	0V
C	–
B	–

Q504R

E	0V
C	–
B	–

Q805

E	4.6V
C	4.3V
B	–

Q503L

E	0V
C	–
B	–

Q505

E	–
C	4.6V
B	0V (4.6V)

Q808

E	–
C	4.3V
B	4.3V

Q503R

E	0V
C	–
B	–

Q508

E	–
C	4.6V
B	–

Q101

E	–
C	–
B	3.3V (0V)

Q502L

E	0V
C	–
B	–

Q502R

E	0V
C	–
B	–

Q501L

E	0V
C	–
B	–

X25-3090-00

U301

1		26	0V	40	
2		27		41	4.5V (0V)
3	2.2V	28	2.3V	42	
4		29		43	0V
5	2.5V	30		44	
6	2.2V	31	3.6V	45	
7	2.5V	32		46	2.2V
8	2.2V			47	
9				48	
10	4.6V	33	4.5V (0V)		
11		34	2.1V (0V)		
12	2.2V	35	4.5V (0V)		
13		36	(0V)		
14	2.8V				
15	2.2V				
16					
17	0.8V	37	4.5V		
18	4.5V (0V)	38	2.2V		
19	0V	39	(0V)		
20					
21	4.5V				
22					
23	4.3V				
24	4.6V				
25	4.5V				

U401

1	(0V)	21	0V	60	
2	4.6V (0V)	22	0V (4.6V)	61	
3	2.1V (0V)	23	(0V)	62	0V
4	(0V)	24	4.6V (0V)	63	
5	(2.2V)	25	4.5V	64	0V
6	4.6V	26		65	
7	4.5V (0V)	27		66	
8		28	4.5V (0V)	67	0V (4.6V)
9		29	–	68	
10		32		69	
11	0V	33	4.5V	70	
12		34	–	71	4.6V
13	4.5V	50		72	0V (4.6V)
14	4.6V	51		73	4.6V
15	4.3V	52	0V	74	0V (4.6V)
16	4.5V	53		75	
17	0V	54		76	
18	4.5V (0V)	55	4.6V	77	
19	0V (4.6V)	58	0V		
20	3.0V (0V)	59			

U403

1	0V	21	4.6V
2	0V (4.6V)	22	4.5V
3	4.6V	23	
4	4.5V (0V)	24	0V
5	4.6V	25	
6	0V	26	4.6V
7		27	
8	(0V)	28	4.3V
		29	4.6V
		30	
9	0V	31	-
10	0V (4.6V)	54	
11	0V	55	3.7V
12		56	2.8V
13		57	1.9V
14	4.6V	58	4.6V
15		59	0V
16		60	
17	4.6V (0V)		
18	4.5V (0V)		
19	0.5V	61	
20	1.4V	62	4.5V
		63	0V
		64	0V

Q301

E	2.2V
C	–
B	–

Q302

E	2.2V
C	–
B	–

Q3002

E	2.2V
C	–
B	–

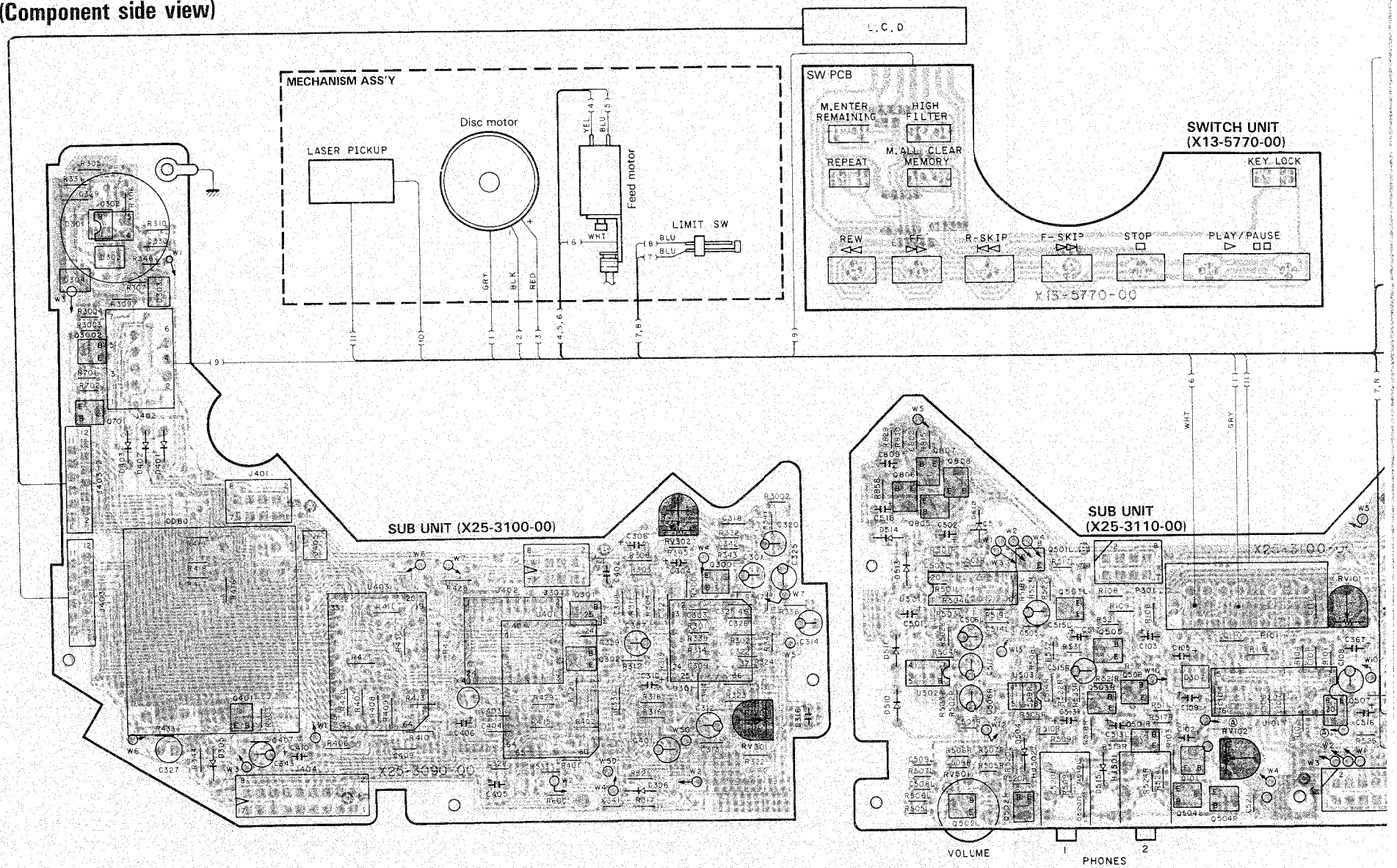
Q701

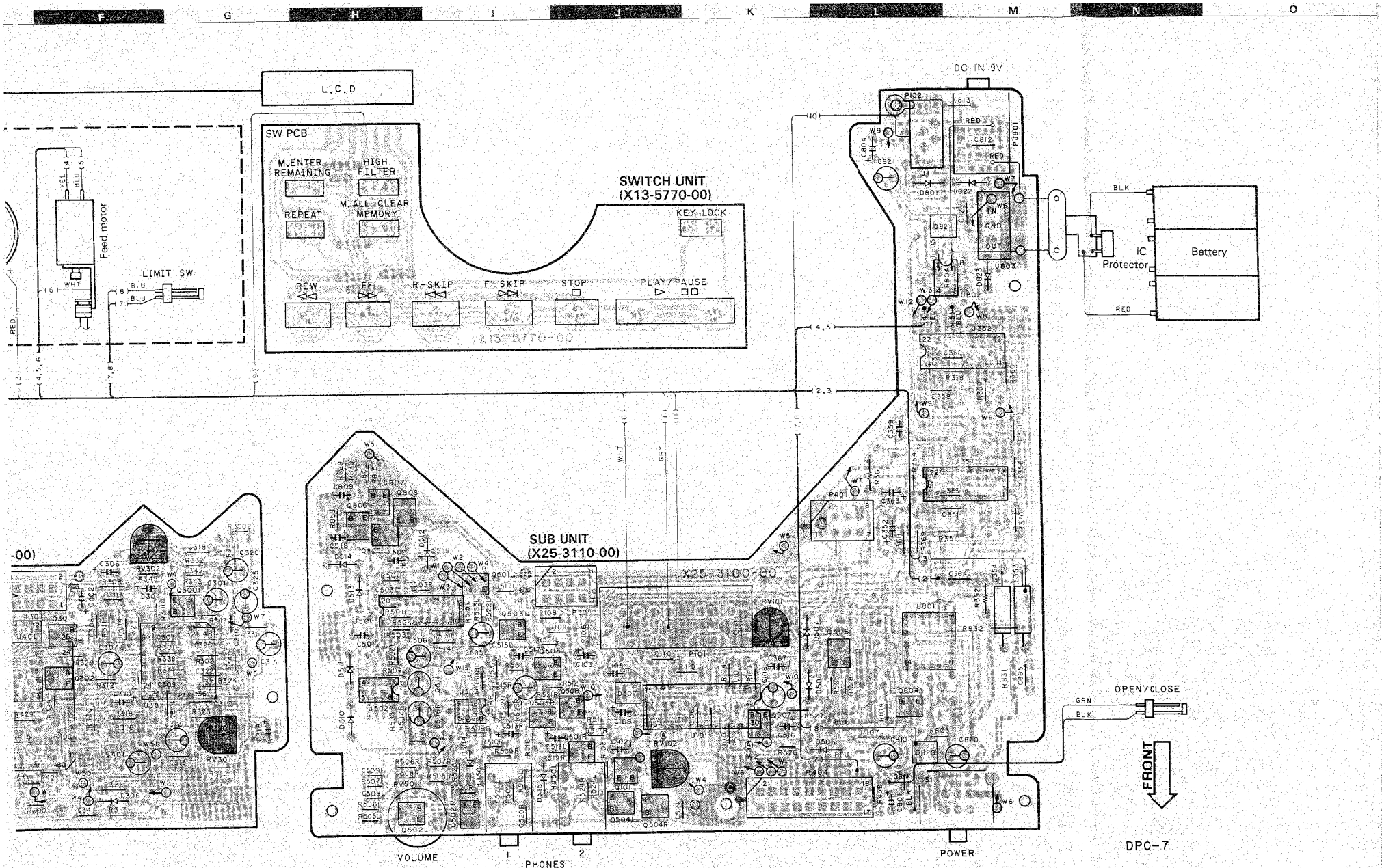
E	
C	4.6V
B	–

Q401

E	4.6V
C	4.5V
B	–

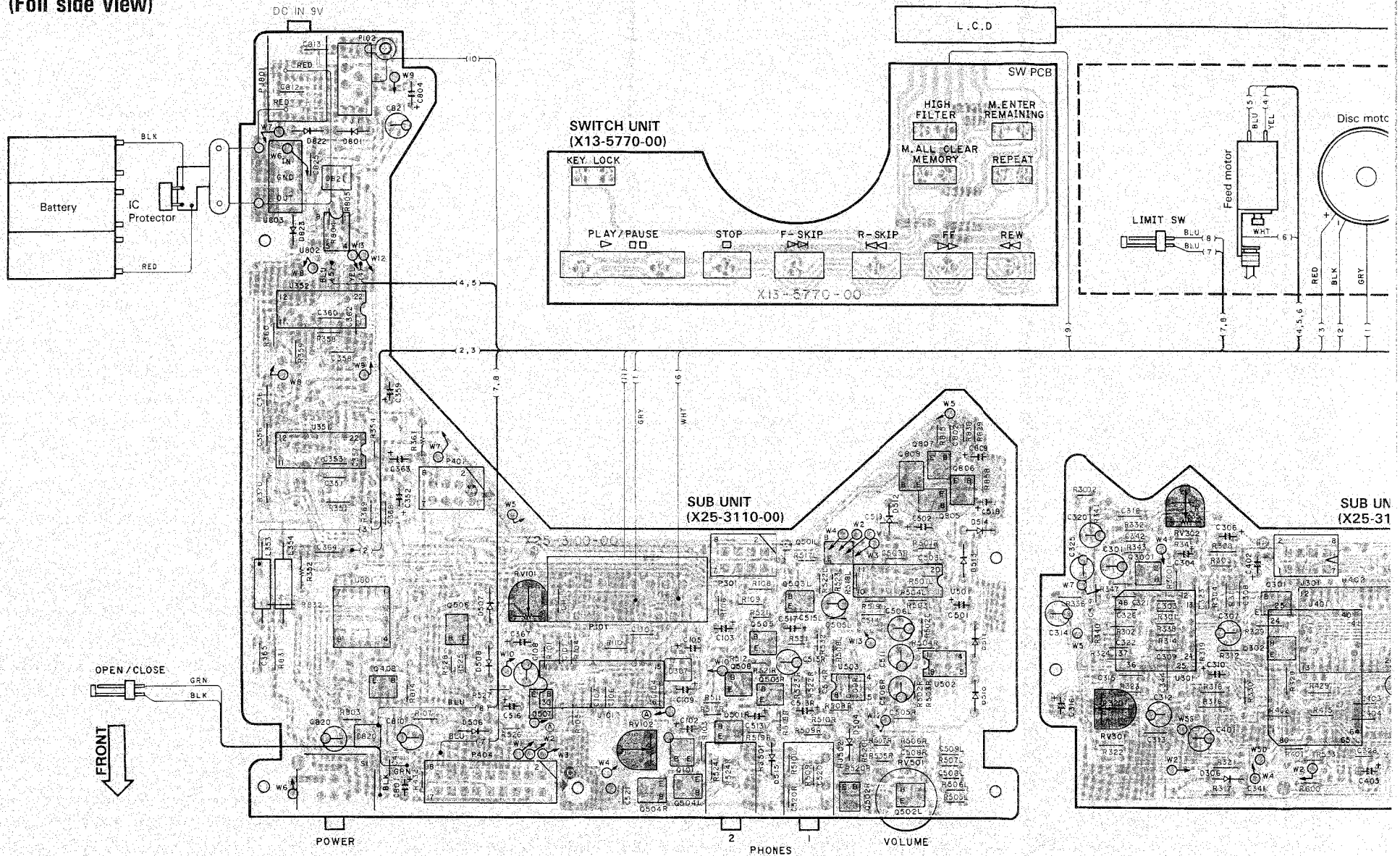
PC BOARD (Component side view)

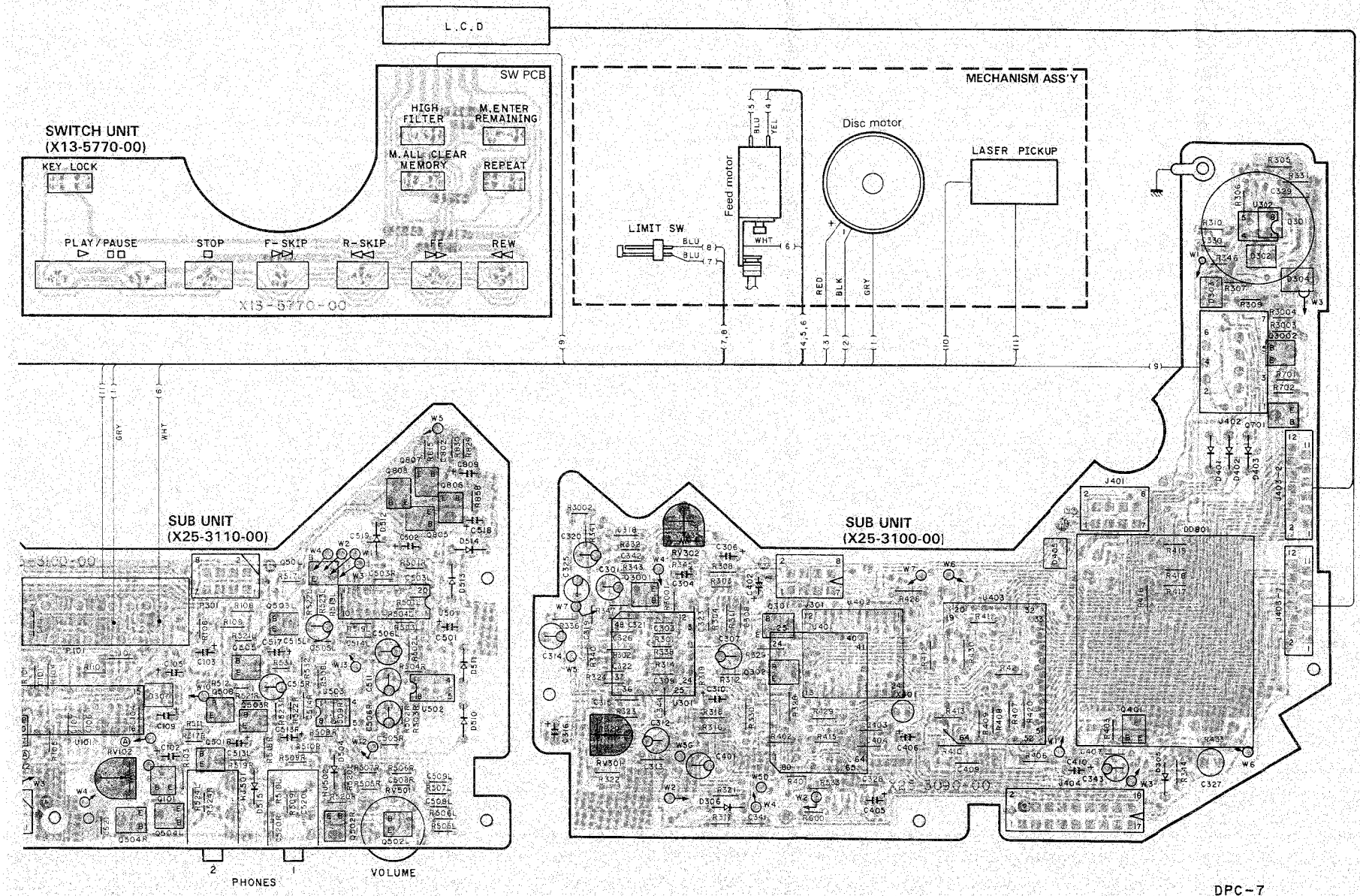




Refer to the schematic diagram for the values of resistors and capacitors.

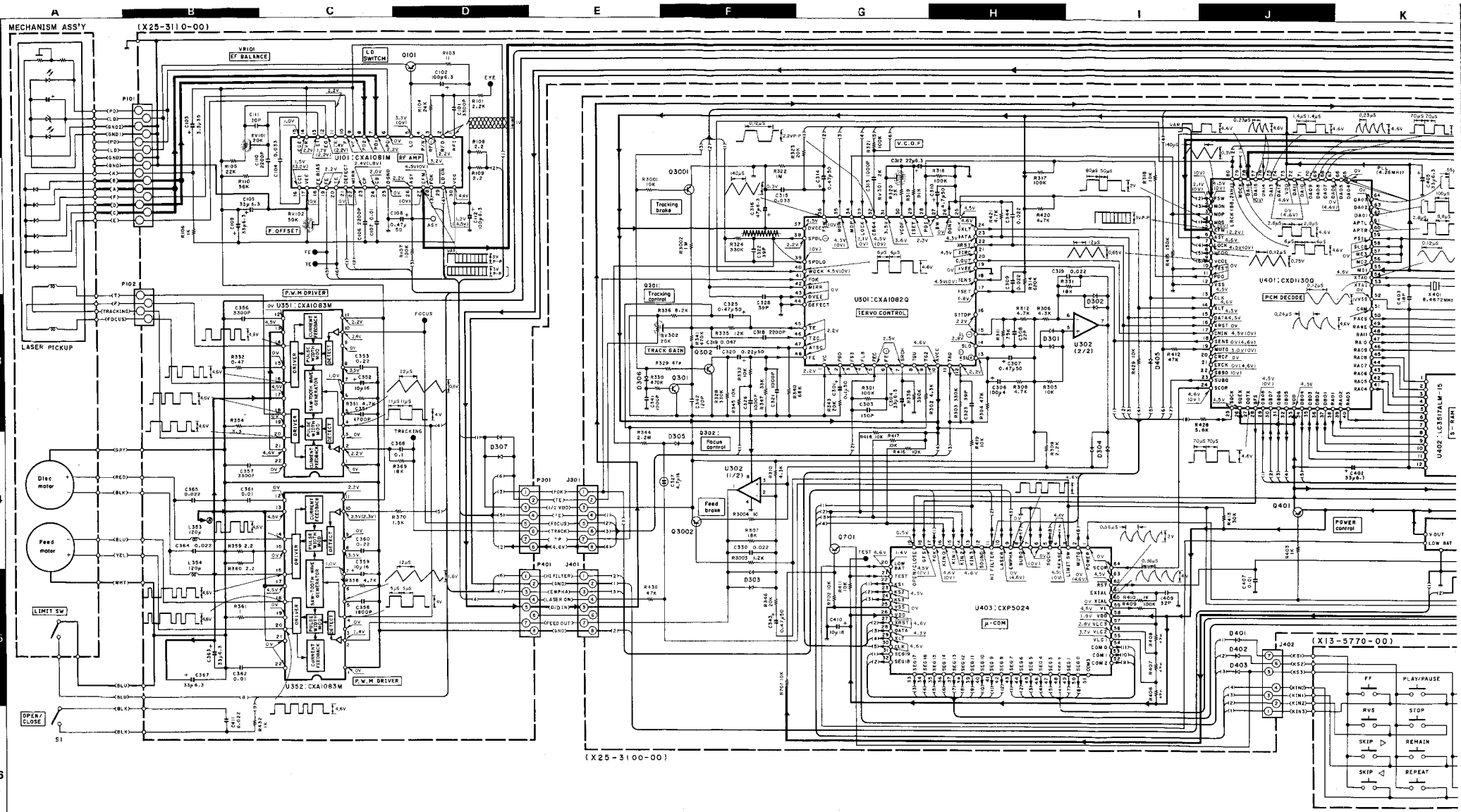
PC BOARD (Foil side view)





DPC-7

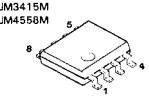
Refer to the schematic diagram for the values of resistors and capacitors.



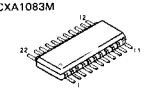
2SB709
2SB970
2SD601

2SB766

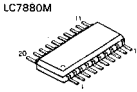
NJM3415M
NJM4558M



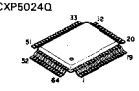
CXA1083M



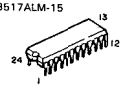
LC7880M



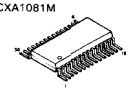
CXP5024Q



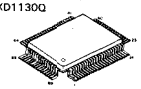
LC3517ALM-15



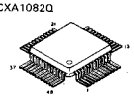
CXA1081M

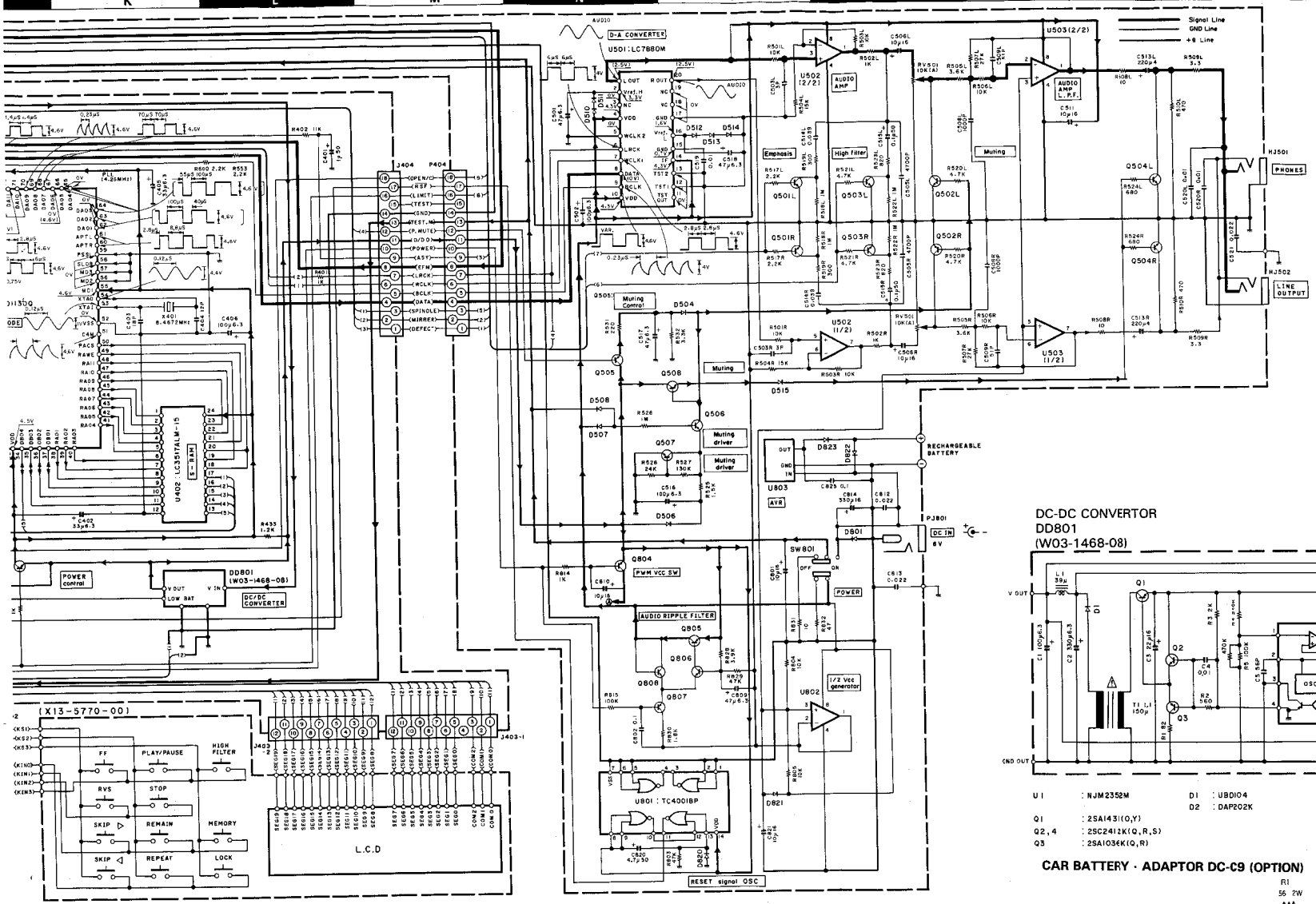


CXD1130Q



CXA1082Q





CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

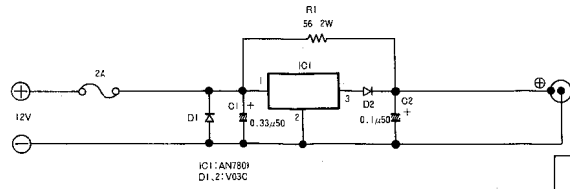
Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Spannungsmesser gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u.U. geringfügig.

DC-DC CONVERTOR
DD801
(W03-1468-08)

U1	: NJM2352M	D1	: UB0104
		D2	: DAP202K
Q1	: 2SA1431(O,Y)		
Q2,4	: 2SC2412K(Q,R,S)		
Q3	: 2SA1036K(Q,R)		

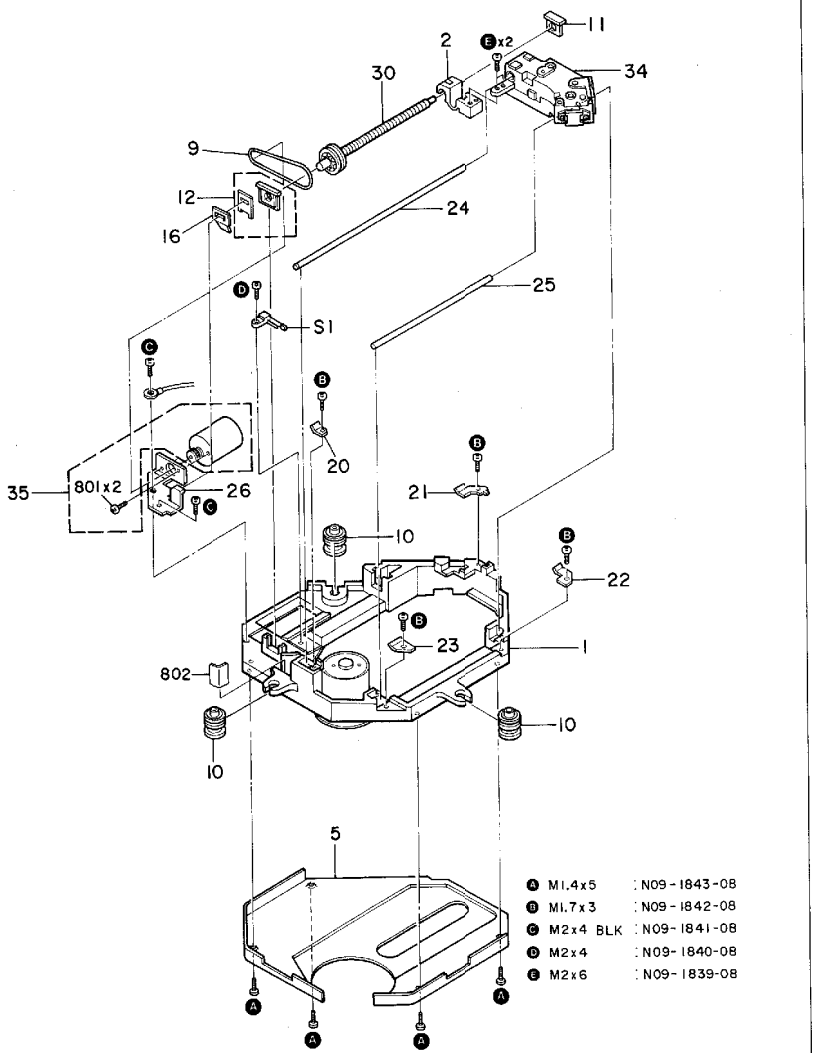
CAR BATTERY · ADAPTOR DC-C9 (OPTION)



U101	: CXA1081M		Q101, 506, 805, 807, 3002	: 2SB709(R,S)	
U301	: CXA1082Q		Q301, 302, 701, 3001	: 2SD601(R,S)	
U302, 503	: NJM3415M		Q401	: 2SB970(R,S)	
U351, 352	: CXA1083M		Q501L, 501R, 502L, 502R, 503L, 503R, 504L, 504R	: 2SD601(R,S)	
U401	: CXD1139Q		505, 507, 508, 806, 808	: 2SB766(R,S)	
U402	: LC3517ALM-15		Q804		
U403	: CXP50240				
U501	: LC7880M		D301 ~ 304, 307	: MA153	
U502, 802	: NJM4558M		D305, 306, 401 ~ 403, 504 ~ 508, 510 ~ 514, 821	: US1040MTA	
U801	: TC4001BP		D405, 820	: MA151K	
U803	: NJM7808		D801, 822, 823	: MPG-06G	

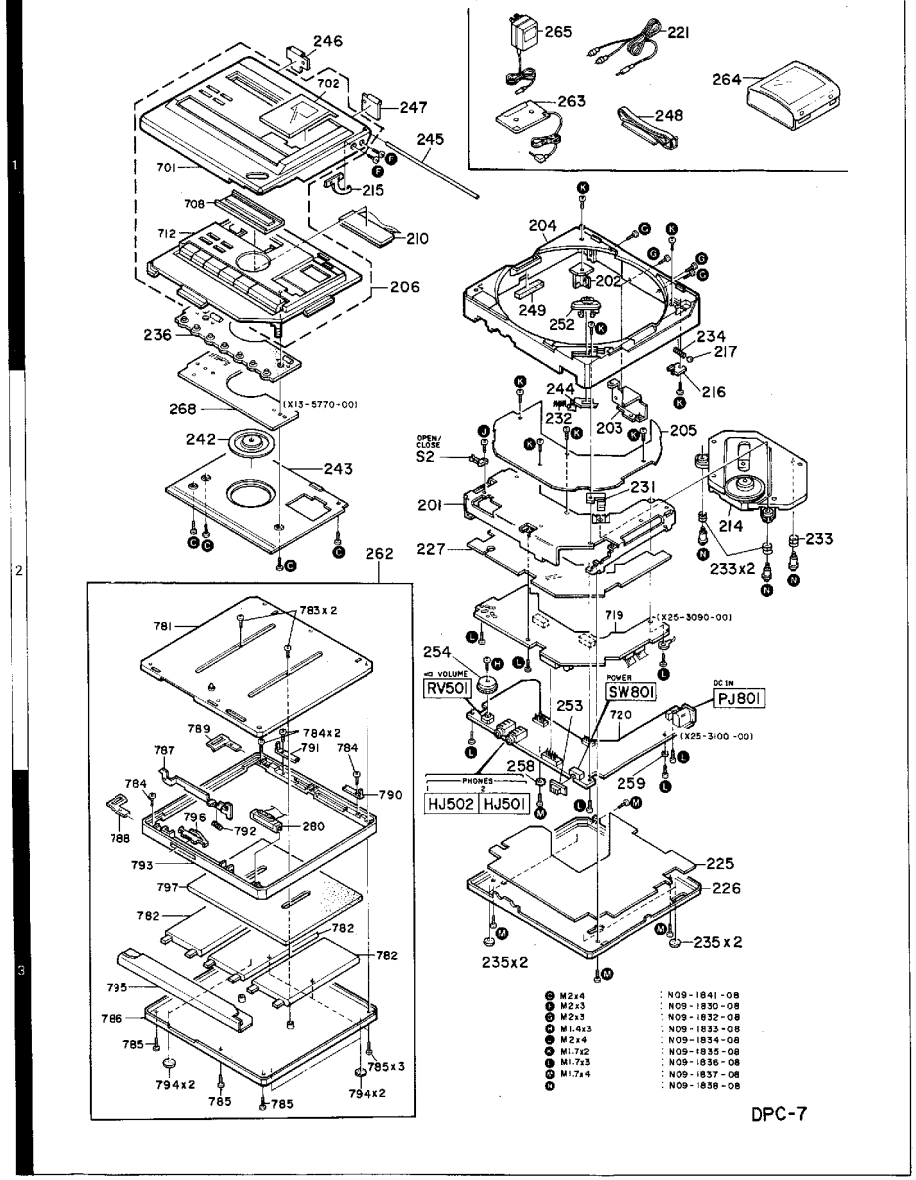
DPC-7
KENWOOD

EXPLODED VIEW (MECHANISM)



Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Telle ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Destination 仕向	Remarks 備考
DPC-7						
201	2C	*	A10-1093-08	CHASSIS		
202	1D	*	A10-1094-08	CHASSIS		
203	2D	*	A10-1095-08	CHASSIS		
204	1D	*	A13-1080-08	FRAME ASSY		
205	2D	*	A15-0057-08	FRAME		
206	1C	*	A20-5353-08	PANEL ASSY		
210	1C	*	B12-0069-08	INDICATOR ASSY (LCD)		
-			B46-0103-14	WARRANTY CARD		
-		*	B50-6925-00	INSTRUCTION MANUAL	K	
-		*	B50-6927-00	INSTRUCTION MANUAL	M	
-		*	B50-6928-00	INSTRUCTION MANUAL	U	
-		*	B50-6929-00	INSTRUCTION MANUAL	E	
-		*	B50-8614-00	INSTRUCTION MANUAL(CAC-1)		
214	2D	*	D40-0579-08	MECHANISM ASSY		
215	1C	*	D10-2010-08	ARM		
216	2D	*	D32-0165-08	STOPPER (BALL)		
217	1D	*	D90-0030-08	BEARING		
221	1D	*	E30-2243-05	AUDIO CORD (15CM)		
226	3D	*	F07-0519-08	COVER (BOTTOM CASE)		
227	2C	*	F19-0551-08	BLIND PLATE		
231	2D	*	G01-2097-08	FLAT SPRING (CASSETTE LID)		
232	2D	*	G01-2098-08	COMPRESSION SPRING(KNOB OPEN)		
233	2D	*	G01-2099-08	COMPRESSION SPRING(DAMPER)		
234	1D	*	G01-2100-08	COMPRESSION SPRING(LID)		
235	3D	*	G11-1227-08	CUSHION (FOOT)		
236	1C	*	G16-0159-08	RUBBER SHEET (SW)		
-		*	G13-0208-08	CUSHION (UPPER)		
-		*	G13-0209-08	CUSHION (BOTTOM)		
-		*	H01-7668-08	ITEM CARTON BOX		
-		*	H25-0296-08	PROTECTION BAG		
-		*	H25-0297-08	PROTECTION BAG		
242	2C	*	J19-2864-08	HOLDER ASSY		
243	2C	*	J19-2865-08	HOLDER		
244	2D	*	J19-2867-08	HOLDER (KNOB OPEN)		
245	1C	*	J19-2868-08	HOLDER (SHAFT)		
246	1C	*	J50-0128-08	HINGE (L)		
247	1C	*	J50-0129-08	HINGE (R)		
248	1D	*	J61-0080-08	SHOULDER BELT ASSY		
249	1D	*	J30-0231-08	SPACER		
252	1D	*	K27-1802-08	KNOB(BUTTON) OPEN/LOCK		
253	2D	*	K27-1803-08	KNOB(BUTTON) POWER		
254	2C	*	K27-1804-08	KNOB(BUTTON) VOLUME		
258	2D	*	N19-1088-08	FLAT WASHER (M2)		
259	3D	*	N19-1089-08	FLAT WASHER (M2)		
C	2C	*	N09-1841-08	SCREW (M2X4)		
F	1C	*	N09-1830-08	SCREW (M2X3)ARM		
G	1D	*	N09-1832-08	SCREW (M2X3)		
H	2D	*	N09-1833-08	SCREW (M1.4X3)		
J	2D	*	N09-1834-08	SCREW (M2X4)		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Telle ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Destination 仕向	Remarks 備考
K	1D,2D	*	N09-1835-08	SCREW (M1.7X2)		
L	2D,3D	*	N09-1836-08	SCREW (M1.7X3)		
M	3D	*	N09-1837-08	SCREW (M1.7X4)		
N	2D	*	N09-1838-08	SCREW (DAMPER)		
S2	2C	*	S46-1100-08	LEAF SWITCH (OPEN/CLOSE)		
262	2C	*	W01-0152-08	BATTERY PACK		
263	1D	*	W01-0153-05	CAR CASSETTE ADAPTOR		
264	1D	*	W03-1437-05	CARRYING CASE		
265	1D	*	W09-0051-08	AC ADAPTOR	K	
265	1D	*	W09-0052-08	AC ADAPTOR	MU	
265	1D	*	W09-0053-08	AC ADAPTOR	E	
268	2C	*	X13-5770-00	SUB-CIRCUIT UNIT		
SUB UNIT (X25-3100-00)						
C301		*	C90-1531-08	ELECTRO 0.1UF 50WV		
C303		*	C90-1537-08	CHIP C 150PF 50WV		
C304		*	C90-1525-08	ELECTRO 33UF 6.3WV		
C306		*	C90-1522-08	ELECTRO 100UF 4WV		
C307		*	C90-1530-08	ELECTRO 0.47UF 50WV		
C308		*	C90-1543-08	CHIP C 22PF K		
C309		*	C90-1545-08	CHIP C 0.022UF K		
C310		*	C90-1533-08	ELECTRO 4.7UF 50WV		
C312		*	C90-1524-08	ELECTRO 22UF 6.3WV		
C313		*	C90-1539-08	CHIP C 1000PF 50WV		
C314		*	C90-1530-08	ELECTRO 0.47UF 50WV		
C315		*	C90-1546-08	CHIP C 0.033UF 50WV		
C316		*	C90-1526-08	ELECTRO 47UF 6.3WV		
C318		*	C90-1544-08	CHIP C 2200PF K		
C319		*	C90-1534-08	CHIP C 0.047UF 25WV		
C320		*	C90-1529-08	ELECTRO 0.22UF 50WV		
C321		*	C90-1539-08	CHIP C 1000PF 50WV		
C322		*	C90-1538-08	CHIP C 39PF 50WV		
C323		*	C90-1547-08	CHIP C 39PF 50WV		
C325		*	C90-1530-08	ELECTRO 0.47UF 50WV		
C326		*	C90-1539-08	CHIP C 1000PF 50WV		
C327		*	C90-1528-08	ELECTRO 4.7UF 16WV		
C328		*	C90-1538-08	CHIP C 39PF 50WV		
C329,330		*	C90-1545-08	CHIP C 0.022UF K		
C341		*	C90-1535-08	CHIP C 1000PF 50WV		
C342		*	C90-1536-08	CHIP C 120PF 50WV		
C343		*	C90-1530-08	ELECTRO 0.47UF 50WV		
C344		*	C90-1545-08	CHIP C 0.022UF K		
C401		*	C90-1532-08	ELECTRO 1UF 50WV		
C402		*	C90-1525-08	ELECTRO 33UF 6.3WV		
C403		*	C90-1542-08	CHIP C 18PF 50WV		
C404		*	C90-1541-08	CHIP C 12PF 50WV		
C405		*	C90-1525-08	ELECTRO 33UF 6.3WV		
C406		*	C90-1523-08	ELECTRO 100UF 6.3WV		
C407		*	C90-1540-08	CHIP C 0.01UF 50WV		
C409		*	C90-1548-08	CHIP C 82PF K		
C410		*	C90-1527-08	ELECTRO 10UF 16WV		
X401		*	L71-0025-08	CRYSTAL FILTER (8.4672MHZ)		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
R301		*	RD73FB1J104J	CHIP R 100K J 1/16W		
R302		*	RD73EB2B432J	CHIP R 4.3K J 1/8W		
R303		*	RD73FB1J334J	CHIP R 330K J 1/16W		
R304			RD73EB2B473J	CHIP R 47K J 1/8W		
R305			RD73EB2B103J	CHIP R 10K J 1/8W		
R306		*	RD73EB2B432J	CHIP R 4.3K J 1/8W		
R307		*	RD73FB1J183J	CHIP R 18K J 1/16W		
R308			RD73EB2B472J	CHIP R 4.7K J 1/8W		
R309		*	RD73FB1J222J	CHIP R 2.2K J 1/16W		
R310		*	RD73EB2B432J	CHIP R 4.3K J 1/8W		
R311		*	RD73EB2B573J	CHIP R 57K J 1/8W		
R312			RD73EB2B472J	CHIP R 4.7K J 1/8W		
R314		*	RD73FB1J624J	CHIP R 620K J 1/16W		
R316		*	RD73EB2B104J	CHIP R 100K J 1/8W		
R317		*	RD73FB1J104J	CHIP R 100K J 1/16W		
R318			RD73EB2B103J	CHIP R 10K J 1/8W		
R319		*	RD73EB2B913J	CHIP R 91K J 1/8W		
R320		*	RD73EB2B302J	CHIP R 3.0K J 1/8W		
R321		*	RD73EB2B104J	CHIP R 100K J 1/8W		
R322			RD73EB2B105J	CHIP R 1.0M J 1/8W		
R323		*	RD73EB2B203J	CHIP R 20K J 1/8W		
R324		*	RD73FB1J334J	CHIP R 330K J 1/16W		
R328			RD73EB2B334J	CHIP R 330K J 1/8W		
R329			RD73EB2B473J	CHIP R 47K J 1/8W		
R330		*	RD73EB2B474J	CHIP R 470K J 1/8W		
R331		*	RD73EB2B183J	CHIP R 18K J 1/8W		
R332		*	RD73FB1J103J	CHIP R 10K J 1/16W		
R335			RD73EB2B123J	CHIP R 12K J 1/8W		
R336		*	RD73EB2B822J	CHIP R 8.2K J 1/8W		
R338		*	RD73FB1J394J	CHIP R 390K J 1/16W		
R340		*	RD73FB1J683J	CHIP R 68K J 1/16W		
R341		*	RD73FB1J474J	CHIP R 470K J 1/16W		
R343		*	RD73FB1J203J	CHIP R 20K J 1/16W		
R344		*	RD73EB2B225J	CHIP R 2.2M J 1/8W		
R345		*	RD73FB1J103J	CHIP R 10K J 1/16W		
R346		*	RD73FB1J203J	CHIP R 20K J 1/16W		
R347		*	RD73FB1J333J	CHIP R 33K J 1/16W		
R401		*	RD73FB1J102J	CHIP R 1.0K J 1/16W		
R402		*	RD73EB2B113J	CHIP R 11K J 1/8W		
R403			RD73EB2B102J	CHIP R 1.0K J 1/8W		
R406-408			RD73EB2B473J	CHIP R 47K J 1/8W		
R409		*	RD73EB2B104J	CHIP R 100K J 1/8W		
R410			RD73EB2B102J	CHIP R 1.0K J 1/8W		
R411			RD73EB2B103J	CHIP R 10K J 1/8W		
R412			RD73EB2B473J	CHIP R 47K J 1/8W		
R413		*	RD73EB2B303J	CHIP R 30K J 1/8W		
R415		*	RD73EB2B154J	CHIP R 150K J 1/8W		
R416-419			RD73EB2B103J	CHIP R 10K J 1/8W		
R420,421			RD73EB2B472J	CHIP R 4.7K J 1/8W		
R428		*	RD73EB2B562J	CHIP R 5.6K J 1/8W		
R429			RD73EB2B103J	CHIP R 10K J 1/8W		
R430			RD73EB2B473J	CHIP R 47K J 1/8W		
R433		*	RD73FB1J122J	CHIP R 1.2K J 1/16W		
R533		*	RD73FB1J222J	CHIP R 2.2K J 1/16W		
R600		*	RD73FB1J222J	CHIP R 2.2K J 1/16W		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Telle ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
R3001		*	RD73FB1J103J	CHIP R 10K J 1/16W		
R3002		*	RD73FB1J105J	CHIP R 1.0M J 1/16W		
R3003		*	RD73FB1J122J	CHIP R 1.2K J 1/16W		
R3004		*	RD73FB1J100J	CHIP R 10 J 1/16W		
RV301		*	R12-1096-08	TRIMMING POT(1K)VOL		
RV302		*	R12-3142-08	TRIMMING POT(20K) TR GAIN		
D301-304		*	MA153	CHIP DIODE		
D305,306		*	US1040MTA	DIODE		
D401-403		*	US1040MTA	DIODE		
D405			MA151K	CHIP DIODE		
Q301,302		*	2SD601(R,S)	TRANSISTOR		
Q401		*	2SB970(R,S)	TRANSISTOR		
Q701		*	2SD601(R,S)	TRANSISTOR		
Q701		*	2SD601(R,S)	TRANSISTOR		
Q3001		*	2SD601(R,S)	TRANSISTOR		
Q3002		*	2SB709(R,S)	TRANSISTOR		
U301		*	CXA1082Q	IC(SERVO SIGNAL PROCESSOR)		
U302		*	NJM3415M	IC(AUDIO AMP)		
U401			CXD1130Q	IC(DIGITAL SIGNAL PROCESSOR)		
U402		*	LC3517ALM-15	IC(2KX8 RAM)		
U403		*	CXP50240	IC(MICROPROCESSOR)		
DD801		*	W03-1468-08	ELECTRIC CIRCUIT MODULE		
SUB UNIT (X25-3110-00)						
C101		*	C90-1573-08	CHIP C 330PF 50WV		
C102		*	C90-1552-08	ELECTRO 100WV 6.3WV		
C103		*	C90-1559-08	ELECTRO 3.3UF 35WV		
C104		*	C90-1566-08	CHIP C 0.033UF 25WV		
C105		*	C90-1576-08	TANTAL 33UF 6.3WV		
C106		*	C90-1570-08	CHIP C 2200PF K		
C107		*	C90-1567-08	CHIP C 0.01UF 50WV		
C108		*	C90-1556-08	ELECTRO 0.47UF 50WV		
C109		*	C90-1576-08	TANTAL 33UF 6.3WV		
C110		*	C90-1570-08	CHIP C 2200PF K		
C111		*	C90-1572-08	CHIP C 30PF K		
C112		*	C90-1550-08	TANTAL 100UF 6.3WV		
C351		*	C90-1575-08	CHIP C 4700PF 50WV		
C352		*	C90-1555-08	ELECTRO 10UF 16WV		
C353		*	C90-1565-08	CHIP C 0.22UF 25WV		
C356,357		*	C90-1573-08	CHIP C 330PF 50WV		
C358		*	C90-1569-08	CHIP C 1800PF K		
C359		*	C90-1555-08	ELECTRO 10UF 16WV		
C360		*	C90-1565-08	CHIP C 0.22UF 25WV		
C361,362		*	C90-1567-08	CHIP C 0.01UF 50WV		
C363		*	C90-1576-08	TANTAL 33UF 6.3WV		
C364,365		*	C90-1571-08	CHIP C 0.022UF K		
C367		*	C90-1553-08	ELECTRO 33UF 6.3WV		
C368		*	C90-1568-08	CHIP C 0.1UF 50WV		
C411		*	C90-1562-08	CHIP C 0.022PF 50WV		
C501		*	C90-1554-08	ELECTRO 47UF 6.3WV		
C502		*	C90-1552-08	ELECTRO 100WV 6.3WV		
C503		*	C90-1560-08	CHIP C 3PF 50WV		
C505		*	C90-1564-08	CHIP C 4700PF 50WV		
C506		*	C90-1555-08	ELECTRO 10UF 16WV		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Telle ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Destination 仕向	Remarks 備考
C509		*	C90-1563-08	CHIP C 470PF 50WV		
C511		*	C90-1555-08	ELECTRO 10UF 16WV		
C513		*	C90-1551-08	ELECTRO 220UF 4WV		
C514		*	C90-1574-08	CHIP C 0.039UF K		
C515		*	C90-1557-08	ELECTRO 0.1UF 50WV		
C516		*	C90-1552-08	ELECTRO 100WV 6.3WV		
C517,518		*	C90-1554-08	ELECTRO 47UF 6.3WV		
C519,520		*	C90-1561-08	CHIP C 0.01UF 50WV		
C521		*	C90-1571-08	CHIP C 0.022UF K		
C801		*	C90-1555-08	ELECTRO 10UF 16WV		
C802		*	C90-1568-08	CHIP C 0.1UF 50WV		
C809		*	C90-1554-08	ELECTRO 47UF 6.3WV		
C810		*	C90-1555-08	ELECTRO 10UF 16WV		
C812,813		*	C90-1571-08	CHIP C 0.022UF K		
C814		*	C90-1549-08	ELECTRO 330UF 16WV		
C820		*	C90-1558-08	ELECTRO 4.7UF 50WV		
C821		*	C90-1555-08	ELECTRO 10UF 16WV		
HJ501,502	3D	*	E11-0177-08	PHONE JACK (PHONES)		
PJ801	2D	*	E11-0176-08	DC JACK (DC IN)		
L353,354		*	L39-0151-08	VARIABLE INDUCTOR(120UH)		
R101			RD73EB2B222J	CHIP R 2.2K J 1/8W		
R103		*	RD73FB1J110J	CHIP R 11 J 1/16W		
R104		*	RD73EB2B243J	CHIP R 24K J 1/8W		
R105			RD73EB2B223J	CHIP R 22K J 1/8W		
R106			RD73EB2B102J	CHIP R 1.0K J 1/8W		
R107		*	RD73EB2B104J	CHIP R 100K J 1/8W		
R108,109		*	RD73EB2B2R2J	CHIP R 2.2 J 1/8W		
R110		*	RD73EB2B563J	CHIP R 56K J 1/8W		
R351			RD73EB2B472J	CHIP R 4.7K J 1/8W		
R352		*	RD14DY2E470J	SMALL-RD 47 J 1/4W		
R354		*	RD73EB2B3R3J	CHIP R 3.3 J 1/8W		
R358			RD73EB2B472J	CHIP R 4.7K J 1/8W		
R359,360		*	RD73EB2B2R2J	CHIP R 2.2 J 1/8W		
R361		*	RD14DY2E109J	SMALL-RD 1.0 J 1/4W		
R369		*	RD73EB2B183J	CHIP R 18K J 1/8W		
R370			RD73EB2B152J	CHIP R 1.5K J 1/8W		
R432		*	RD73FB1J102J	CHIP R 1.0K J 1/16W		
R501		*	RD73FB1J103J	CHIP R 10K J 1/16W		
R502		*	RD73FB1J102J	CHIP R 1.0K J 1/16W		
R503		*	RD73FB1J103J	CHIP R 10K J 1/16W		
R504		*	RD73FB1J153J	CHIP R 15K J 1/16W		
R505		*	RD73FB1J362J	CHIP R 3.6K J 1/16W		
R506		*	RD73FB1J103J	CHIP R 10K J 1/16W		
R507		*	RD73FB1J273J	CHIP R 27K J 1/16W		
R508		*	RD73FB1J100J	CHIP R 10 J 1/16W		
R509		*	RD73FB1J3R3J	CHIP R 3.3 J 1/16W		
R510		*	RD73FB1J471J	CHIP R 470 J 1/16W		
R511,512		*	RD73FB1J104J	CHIP R 100K J 1/16W		
R517		*	RD73FB1J222J	CHIP R 2.2K J 1/16W		
R518		*	RD73FB1J105J	CHIP R 1.0M J 1/16W		
R519		*	RD73FB1J301J	CHIP R 300 J 1/16W		
R520,521		*	RD73FB1J472J	CHIP R 4.7K J 1/16W		
R522		*	RD73FB1J105J	CHIP R 1.0M J 1/16W		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

DPC-7

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Telle ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
R523		*	RD73FB1J821J	CHIP R 820 J 1/16W		
R524		*	RD73FB1J681J	CHIP R 680 J 1/16W		
R525		*	RD73FB1J152J	CHIP R 1.5K J 1/16W		
R526		*	RD73FB1J243J	CHIP R 24K J 1/16W		
R527		*	RD73FB1J134J	CHIP R 130K J 1/16W		
R528		*	RD73FB1J105J	CHIP R 1.0M J 1/16W		
R531		*	RD73FB1J221J	CHIP R 220 J 1/16W		
R532		*	RD73FB1J332J	CHIP R 3.3K J 1/16W		
R803		*	RD73FB1J473J	CHIP R 47K J 1/16W		
R804-806		*	RD73FB1J103J	CHIP R 10K J 1/16W		
R814			RD73EB2B102J	CHIP R 1.0K J 1/8W		
R815		*	RD73EB2B104J	CHIP R 100K J 1/8W		
R828			RD73EB2B392J	CHIP R 3.9K J 1/8W		
R829			RD73EB2B473J	CHIP R 47K J 1/8W		
R830		*	RD73EB2B182J	CHIP R 1.8K J 1/8W		
R831			RD73EB2B100J	CHIP R 10 J 1/8W		
R832			RD73EB2B470J	CHIP R 47 J 1/8W		
RV101		*	R12-3143-08	TRIMMING POT. (20K) FE BALANCE		
RV102	2D	*	R12-4033-08	TRIMMING POT. (50K) F. OFFSET		
RV501	2D	*	R29-3025-08	POTENTIOMETER(10K) VOLUME		
SW801	3D	*	S31-0041-08	SLIDE SWITCH (POWER)		
D307		*	MA153	CHIP DIODE		
D504		*	US1040MTA	DIODE		
D506-508		*	US1040MTA	DIODE		
D510		*	US1040MTA	DIODE		
D511-514		*	US1040MTA	DIODE		
D801		*	MPG-06G	DIODE		
D801		*	MPG06G	DIODE		
D820			MA151K	DIODE		
D821		*	US1040MTA	DIODE		
D822,823		*	MPG06G	DIODE		
Q101		*	2SB709	TRANSISTOR		
Q501-505		*	2SD601(R,S)	TRANSISTOR		
Q506		*	2SB709	TRANSISTOR		
Q507,508		*	2SD601(R,S)	TRANSISTOR		
Q804		*	2SB766(R,S)	TRANSISTOR		
Q805		*	2SB709	TRANSISTOR		
Q806		*	2SD601(R,S)	TRANSISTOR		
Q807		*	2SB709	TRANSISTOR		
Q808		*	2SD601(R,S)	TRANSISTOR		
U101		*	CXA1081M	IC(RF AMP)		
U351,352		*	CXA1083M	IC(PWM DRIVER)		
U501		*	LC7880M	IC(D-A CONVERTER)		
U502			NJM4558M	IC(OP AMP X2)		
U503		*	NJM3415M	IC(AUDIO AMP)		
U801			TC4001BP	IC(NOR X6)		
U802			NJM4558M	IC(OP AMP X2)		
MECHANISM ASS'Y (D40-0579-08)						
1	2B	*	A11-0244-08	SUB CHASSIS ASSY(MOTOR)		
2	1B	*	A15-0058-08	FRAME (PICKUP)		
5	3A	*	B07-1759-08	ESCUTCHEON		
9	1A	*	D16-0167-08	BELT (FEED MOTOR)		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Telle ohne **Parts No.** werden nicht geliefert.

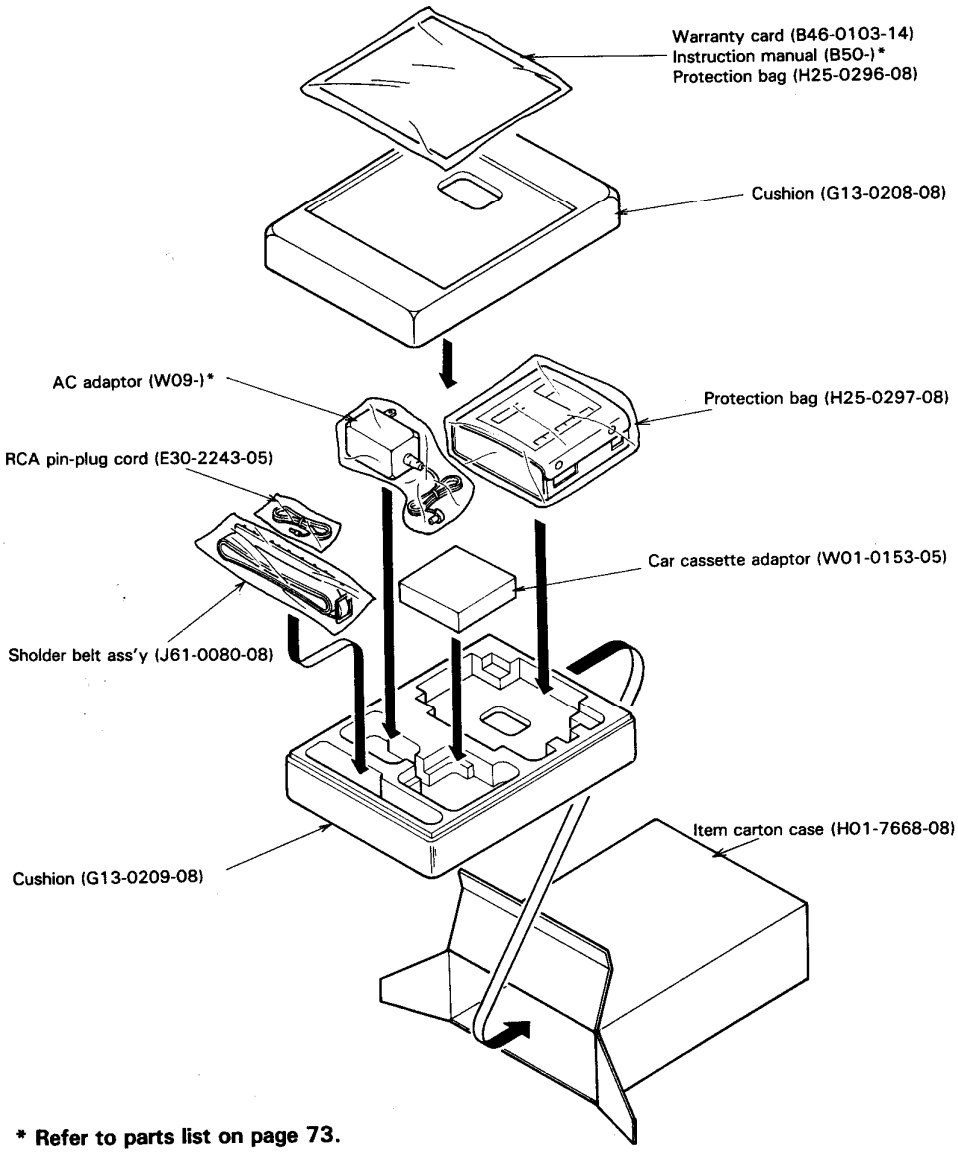
Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
10	2A,2B	*	D39-0188-08	DAMPER		
11		*	D90-0032-08	STEEL BALL		
12	1A	*	D90-0033-08	BEARING		
16	1A	*	G01-2101-08	FLAT SPRING (AZIMUTH)		
20	2A	*	J11-0099-08	CLAMPER (A)		
21	2B	*	J11-0100-08	CLAMPER (B)		
22	2B	*	J11-0101-08	CLAMPER (C)		
23	2B	*	J11-0102-08	CLAMPER (D)		
24	1B	*	J19-2869-08	HØLDER (PU SHAFT)		
25	1B	*	J19-2870-08	HØLDER (PU SHAFT)		
26	2A	*	J19-2872-08	HØLDER (MØTØR)		
30	1B	*	N99-0262-08	FEED SCREW ASSY		
A	3A,3B	*	N09-1843-08	SCREW (M1.4X5)		
B	2B	*	N09-1842-08	SCREW (M1.7X3)		
C	2A	*	N09-1841-08	SCREW (M2X4)		
D	1A	*	N09-1840-08	SCREW (M2X4)		
E	1B	*	N09-1839-08	SCREW (M2X6)		
S1	2A	*	S46-1101-08	LEAF SWITCH (LIMIT).		
34	1B	*	T31-0042-08	PICKUP ASSY (MLP-6)		
35	2A	*	T49-0021-08	FEED MØTØR ASSY		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

DPC-7

PACKING



*** Refer to parts list on page 73.**

KENWOOD CORPORATION
Shionogi Shibuya Building, 17-5, 2-chome Shibuya, Shibuya-ku, Tokyo 150, Japan

KENWOOD U.S.A. CORPORATION
2201 East Dominguez Street, Long Beach, CA 90810;
550 Clark Drive, Mount Olive, NJ 07828, U.S.A.

KENWOOD ELECTRONICS CANADA INC.
P.O. Box 1075 959 Gana Court, Mississauga, Ontario, Canada L4T 4C2

KENWOOD ELECTRONICS BENELUX N.V.
Mechelsesteenweg 418 B-1930 Zaventem, Belgium

KENWOOD ELECTRONICS DEUTSCHLAND GMBH
Rembrucker-Str. 15, 6056 Heusenstamm, West Germany

TRIO-KENWOOD FRANCE S.A.
Hi-Fi·VIDEO·CAR Hi-Fi
13, Boulevard Ney, 75018 Paris, France

TRIO-KENWOOD U.K. LTD.
17 Bristol Road, The Metropolitan Centre, Greenford, Middx. UB6 8UP England

KENWOOD ELECTRONICS AUSTRALIA PTY. LTD.
4E Woodcock Place, Lane Cove, N.S.W. 2066, Australia

KENWOOD & LEE ELECTRONICS, LTD.
Wang Kee Building, 5th Floor, 34-37, Connaught Road, Central, Hong Kong